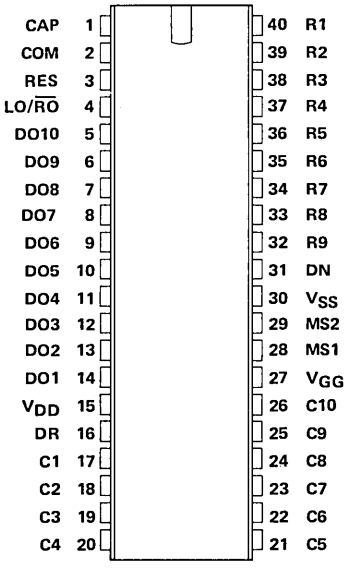
# TMS 5001 NL
# 4-MODE DYNAMIC 90-KEY KEYBOARD ENCODER

BULLETIN NO. DL-S 7512274, MAY 1975

- ASCII Logical Bit-Pairing and Typewriter Codes
- ASR33 Teletype Code
- Baudot Paper Tape Punch Code
- N-Key Roll-Over or Lockout Mode
- Data-Ready Pulsed Output
- Internal Oscillator
- Latched Data Outputs
- Adjustable Key-Noise Protection
- Keyboard Column Leakage Compensation
- Compatible with Reed and Mechanical Switches
- TTL-Compatible Inputs and Outputs
- 10-Bit Output Words

40-PIN PLASTIC
DUAL-IN-LINE PACKAGE
(TOP VIEW)




## description

The TMS 5001 NL is an MOS LSI dynamic encoder for use with standard keyboards having up to 90 keys. The encoder is pre-programmed to generate in positive logic two ANSI-standard codes – the logical bit pairing and the typewriter codes – the ASR33 teletype code, and the Baudot paper tape code. The device utilizes a 3600-bit ROM (40 x 90 organization), a 9-row by 10-column key-scanning matrix, driver and sense amplifier interface circuits, a control circuit, a shift-register memory, and an on-chip oscillator with frequency determined by an external resistor and capacitor.

The circuit can operate in the N-key roll-over or N-key lockout mode with external logic control. Key-make and key-break noise is ignored after initial key identification because scanning is terminated for a time interval that can be adjusted with another external capacitor at the delay-node terminal.

One of four key modes is selected by proper input levels at two mode-select terminals. A data-ready pulse is generated to indicate that a key is depressed, the binary word has been encoded, and that word is available at the I/O terminals.

The control inputs are compatible with Series 74 TTL circuits using pull-up resistors. Each data output can drive one Series 74 TTL circuit without external resistors.

The TMS 5001 NL is offered in a 40-pin dual-in-line plastic (NL suffix) package designed for insertion in mounting-hole rows on 600-mil centers. The device is characterized for operation from 0°C to 70°C.

## operation

The TMS 5001 subsystem consists basically of an oscillator, row and column matrix scanners, a control section with memory, and a ROM with buffered outputs.

### oscillator

The internal oscillator generates two internal clock signals at the oscillator frequency that control the precharge of the column inputs and drive the row and column scanning counters. The oscillator frequency is set by an external resistor connected between the **resistor** (RES) and **common** (COM) terminals and an external capacitor connected between the **capacitor** (CAP) and **common** (COM) terminals.



PRELIMINARY DATA SHEET:
Supplementary data may be published at a later date.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

## operation (continued)

### row and column matrix scanners

The keyboard is connected to the **column** (C1-C10) inputs and the **row** (R1-R9) outputs. During one half of an oscillator cycle, the column inputs and row outputs are precharged to a negative voltage. In the next half-cycle, the modulo-10-counter column scanner enables one of the ten column-input gates and the modulo-9-counter row scanner allows one row to be connected to $V_{SS}$ (nominally 5 V) through an MOS transistor having an impedance of about 600 ohms. If the keyboard switch for that row and column is closed, the column input line capacitance discharges through the MOS load to $V_{SS}$. At a voltage $V_{SH}$ (near $V_{SS}$) the key closure is detected and scanning immediately stops. The row and column position is uniquely identified and stored as a single bit in a 90-bit shift register (see control section). Any single key depression is detected within one keyboard scan cycle, which is 90 oscillator or clock cycles. Within one-half clock cycle after detection, the output word becomes valid at the **data out** (DO1-DO10) terminals.

In the roll-over mode, two clock cycles plus one delay-node interval after detection of a depressed key the scanning operation resumes and the next depressed-key location is detected and stored in the memory. Any new output word becomes valid one-half clock cycle after detection. If multiple keys are depressed simultaneously, the scanners will ultimately locate and store all locations in the memory and each output word will become valid in rapid sequence.

3

In the lockout mode as the delay node voltage drops through $V_{SL}$, scanning does not resume until the first key is released and the first output remains valid until the second depressed key is detected. Thus the second and subsequent depressed keys are ignored until the first key is released.

In either mode when a key is released, scanning in the next cycle is halted when that key location is reached. The halt signal is obtained from the information in the memory identifying that key location. Key-release noise is therefore ignored until the delay node again precharges to $V_{SL}$. Then scanning resumes and the next depressed key is identified and its location stored in the memory.

### control section

The **delay node** (DN) terminal voltage controls the time during which scanning stops after key detection. An external capacitor may be connected between DN and $V_{DD}$ to lengthen this delay. Key-noise immunity can therefore be adjusted according to the key-switch characteristics.

A high-level **data ready** (DR) output pulse having a length of one clock cycle appears one-half clock cycle after the output data becomes valid to indicate that the encoded output word is available at the ten outputs.

The **lockout/roll-over** (LO/$\overline{\text{RO}}$) terminal places the device in the lockout operating mode when the LO/$\overline{\text{RO}}$ input is high or in the roll-over mode when LO/$\overline{\text{RO}}$ is low.

### ROM and output buffers

The row counter output addresses the ROM to generate a unique 10-bit binary word for each of the four modes and each of the 90 key positions. One of the four modes is selected by combinations of high- and low-level inputs at the **mode select** terminals (MS1 and MS2) as shown in the Character Output Charts.

The **data outputs** (DO1-DO8) can drive Series 74 TTL circuits without external resistors. Output data becomes valid within one-half clock cycle after a key is detected.

In the lockout mode, output words are latched and data remains valid until all three of the following events occur: 1) the key is released, 2) the delay node precharges to $V_{SL}$ and scanning starts, and 3) a new key is depressed and detected.

In the roll-over mode, output data remains valid only until the delay node charges to $V_{SL}$ and another key is detected. The DR pulse is generated within one cycle after key detection.



TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

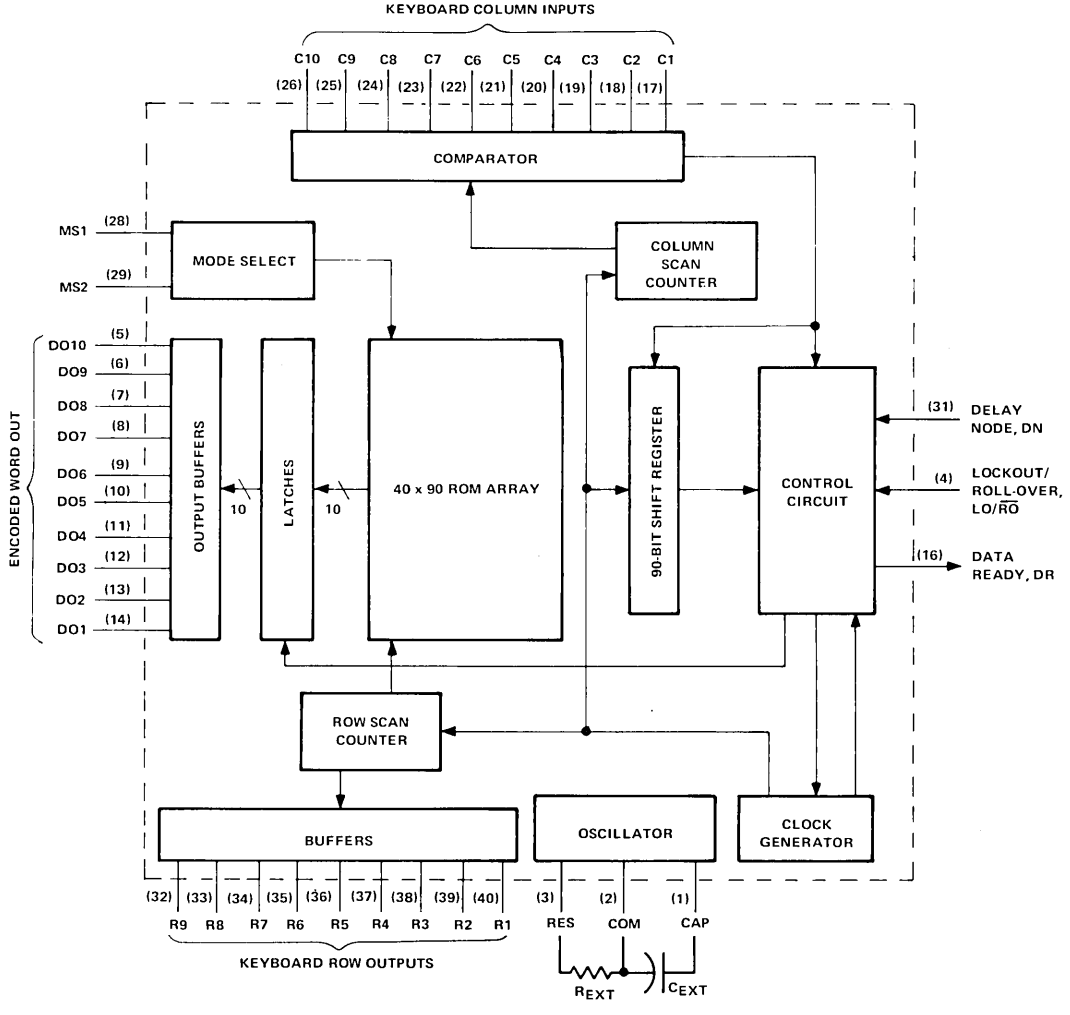
## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)*

| | |
|---|---|
| Supply voltage, $V_{DD}$ (see Note 1) | −20 V to 0.3 V |
| Supply voltage, $V_{GG}$ (see Note 1) | −20 V to 0.3 V |
| Input voltages (all inputs) (see Note 1) | −20 V to 0.3 V |
| Operating free-air temperature range | 0°C to 70°C |
| Storage temperature range | −55°C to 150°C |

NOTE 1: Under absolute maximum ratings, voltage values are with respect to the normally most positive supply, $V_{SS}$ (substrate). Throughout the remainder of this data sheet voltage values are with respect to $V_{DD}$.

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## functional block diagram



## recommended operating conditions

| PARAMETER | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|
| Supply voltage, $V_{DD}$ | | 0 | | V |
| Supply voltage, $V_{GG}$ | −11 | −12 | −13 | V |
| Supply voltage, $V_{SS}$ | 4.75 | 5 | 5.25 | V |
| High-level input voltage (MS and LO/$\overline{RO}$ inputs), $V_{IH}$ | $V_{SS}$ −1.6 | | $V_{SS}$ | V |
| Low-level input voltage (MS and LO/$\overline{RO}$ inputs), $V_{IL}$ | | | $V_{SS}$ −3.9 | V |
| Oscillator frequency, $f_{osc}$ | 10 | | 100 | kHz |
| Operating free-air temperature, $T_A$ | 0 | | 70 | °C |

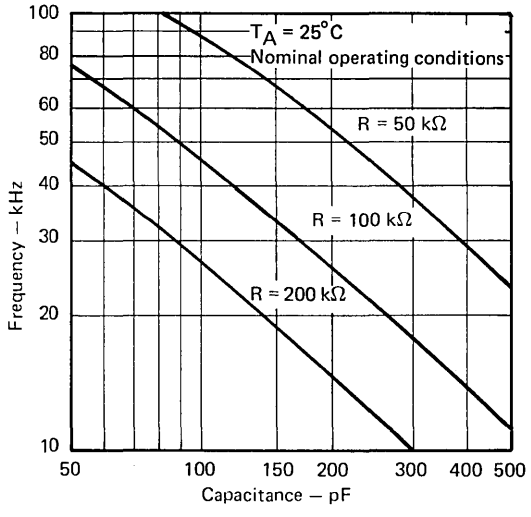
## electrical characteristics over recommended operating free-air temperature range

| PARAMETER | TEST CONDITIONS | MIN | MAX | UNIT |
|---|---|---|---|---|
| High-level sense voltage, $V_{SH}$ | | $V_{SS}$ −2.2 | $V_{SS}$ | V |
| Low-level sense voltage (see Note 2), $V_{SL}$ | | | $V_{SS}$ −7.8 | V |
| High-level output voltage, data ready and DO outputs, $V_{OH}$ | $I_{OH}$ = 100 μA | $V_{SS}$ −1 | $V_{SS}$ | V |
| Low-level output voltage, data ready and DO outputs, $V_{OL}$ | $I_{OL}$ = 1.6 mA | 0 | 0.5 | V |
| Precharge voltage at column inputs (see Note 2) | | | $V_{GG}$ +7.5 | V |
| Supply current from $V_{GG}$, $I_{GG}$ | | | −42 | mA |
| Row or column line capacitance | f = 100 kHz | | 1000 | pF |

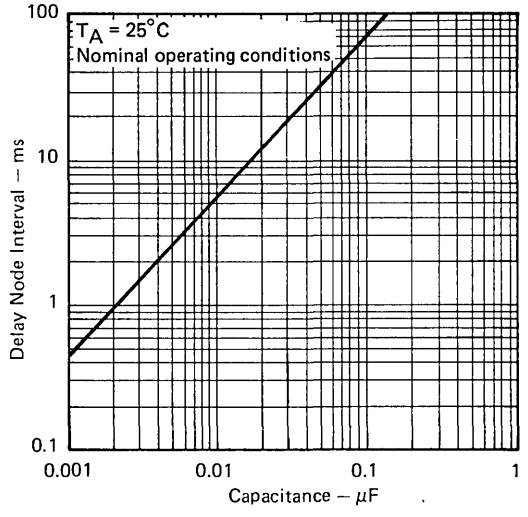
NOTE 2: The algebraic convention where the most positive (least negative) limit is designated as maximum is used in this data sheet for sense and precharge voltage levels only.

## TYPICAL OPERATING CHARACTERISTICS

### OSCILLATOR FREQUENCY vs EXTERNAL RESISTANCE AND CAPACITANCE



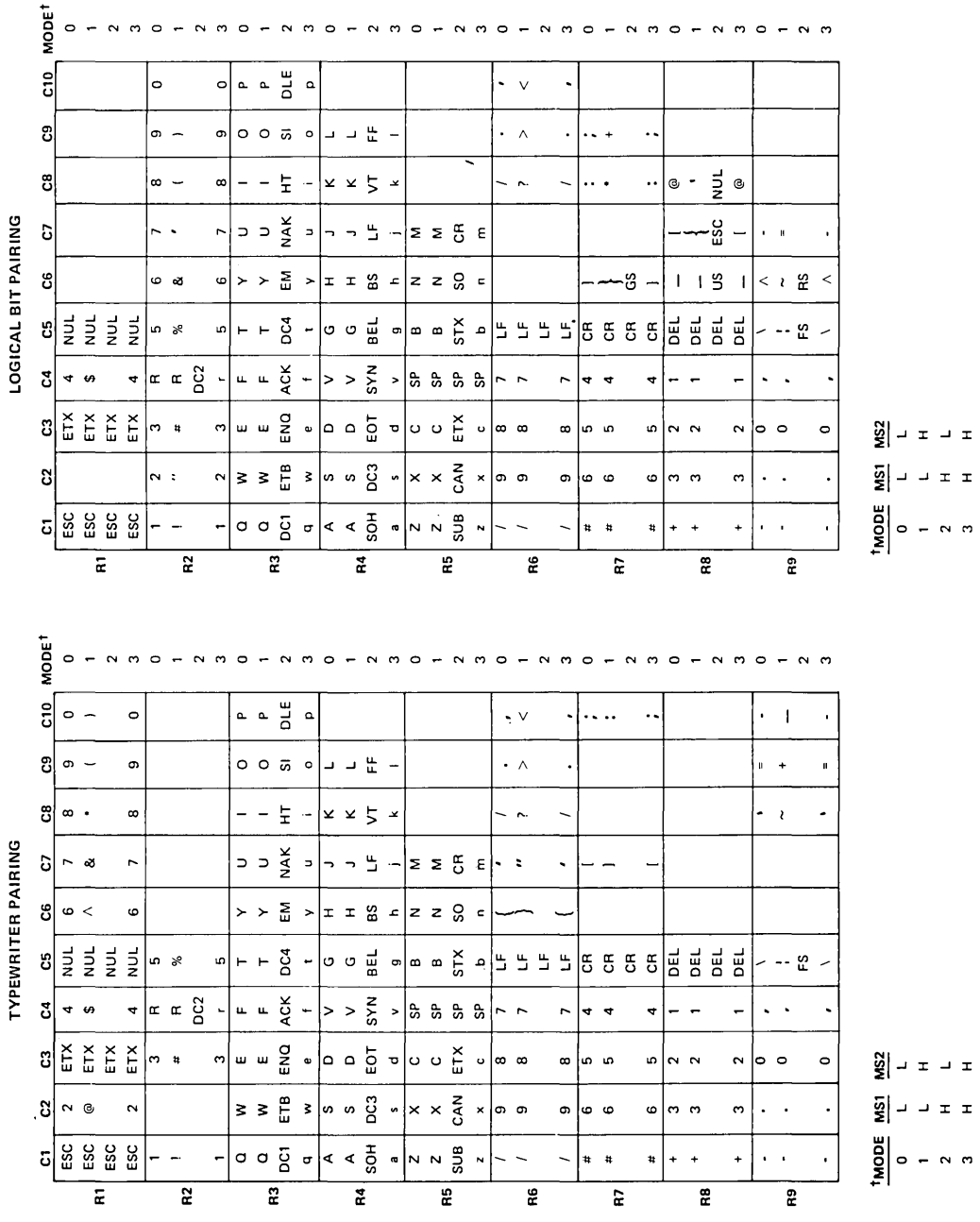

### DELAY NODE INTERVAL vs EXTERNAL CAPACITANCE



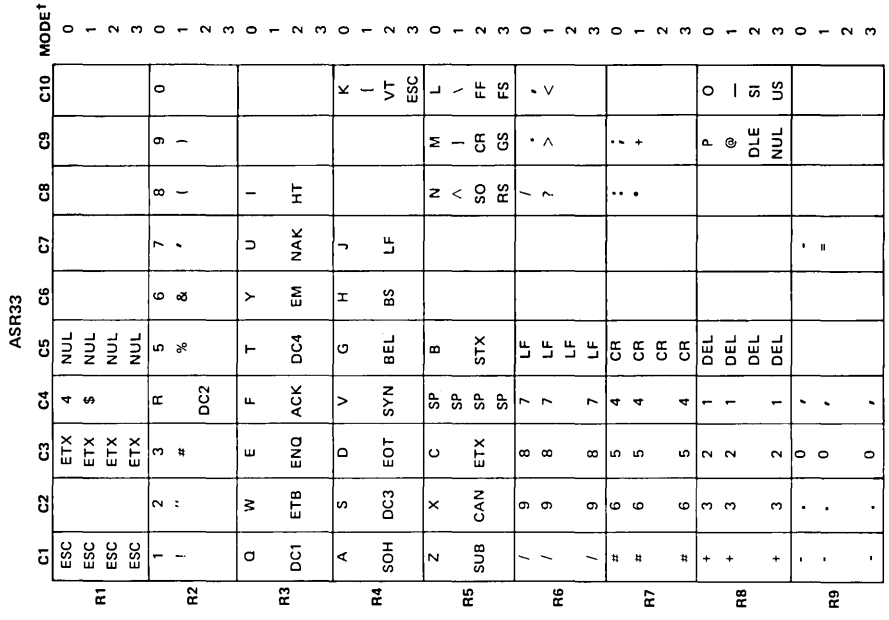


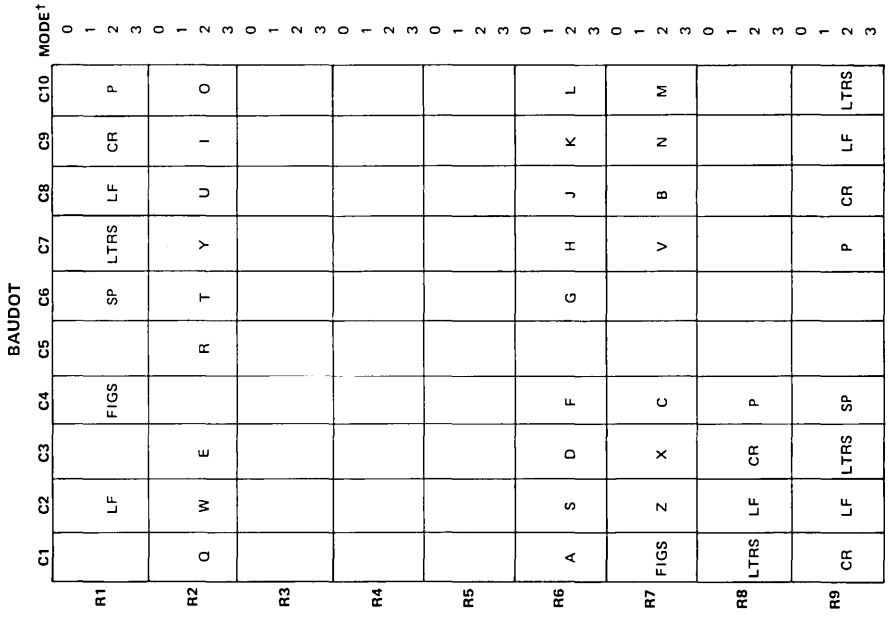

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

## character output charts



## character output charts






TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222