

Capacitive Keyboard Encoder

READ ONLY MEMORY

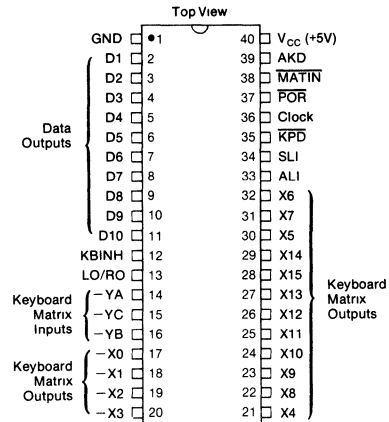
FEATURES

- 128 Key Keyboard Encoder: 112 Fully Decoded Keys, 16 Discrete Function Keys
- 112 Keys With 4 Modes, 10 Bit Output
- Key Validation Logic Protects Against Bounce
- N-Key Roll Over or 2-Key Roll Over
- Internal ROM Allows Any Keys to Control SHIFT CTRL, SHIFT LOCK and ALPHA LOCK
- ALPHA LOCK and SHIFT LOCK Indicator Lines
- Any Key Down (AKD) Strobe
- Single +5 Volt Power Supply
- Programmable Coding of Standard and Special Function Keys
- Zener Diode Protection on All I/O Pins
- Low Power Consumption, Less Than 2 MW per Key
- Usable with Capacitive, Magnetic, Inductive, Hall Effect, or Mechanical Keyboard Switches
- Inputs and Outputs TTL and CMOS Compatible
- Internal Oscillator

DESCRIPTION

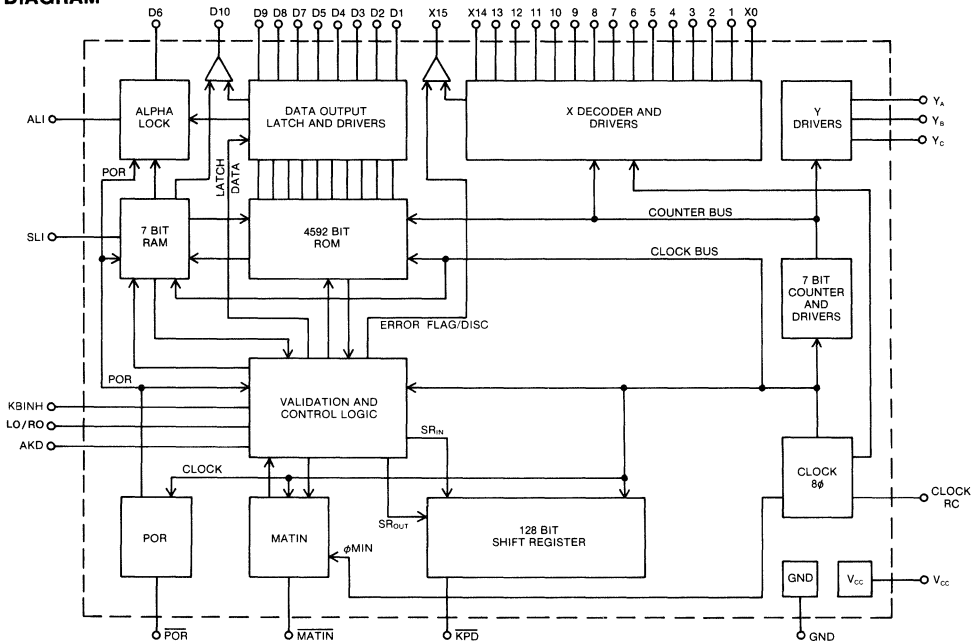
The General Instrument AY-3-4592 is a unique dual pulse scanning encoder and keyboard controller for 112 keys in four modes and 16 programmable discrete function keys. ROM programming permits any keys to control the shift control and lock functions. The AY-3-4592 can be used with capacitive, inductive (magnetic) or switch closure type switches since it works on pulse detection.

PIN CONFIGURATION 40 LEAD DUAL IN LINE



The AY-3-4592 is fabricated with General Instrument N-Channel MOS technology on a single chip containing a 4592 bit ROM, a 128 bit shift register and an internal oscillator.

BLOCK DIAGRAM



PIN FUNCTIONS

READ ONLY MEMORY

Pin No.	Name	Symbol	Function																																		
1	Ground	GND	Ground Pin																																		
2-10	Data Out	D1-D9	Data Outputs, D1 through D9																																		
11	Data Out	D10	Data Output D10. See AY-3-4592 options for complete description																																		
12	Key Inhibit	KBINH	Logic "1" on KBINH will inhibit the processing of Key closures and prevent new output codes. See AY-3-4592 options for other custom options.																																		
13	Lockout/rollover	LO/RO	High for 2 Key Rollover operation, low for N Key Rollover operation. This input is a high impedance Schmitt trigger with thresholds of approximately ¼ (low) and ¾ (high) of V _{CC} . This allows easy interfacing with very slow RC circuits for such functions as "repeat delay". LO/RO is internally "anded" with AKD/STB; if either is low, N Key rollover is automatically selected.																																		
14-16	Y-Address	YA, YB, YC	Y Address lines select one of eight Y inputs through external multiplexer. Scan sequence is Y7 to Y0																																		
17-27, 30-32	X Outputs	X0-X13, X5-X7	X output drivers for Matrix scanning. Scan sequence is X15 to X0. Each driver generates 8 pairs of pulses each scanning cycle.																																		
28, 29	X15, 14	X15, X14	X15 is programed as a "discrete output" key in the standard part. Optionally it may be programed as an error flag or as a Matrix drive line. See AY-3-4592 options. Unlike X0-X13, neither X14 nor X15 have associated ROM output codes. These lines are used to enable separate discrete keys to be debounced using an addressable latch as illustrated in figure 2.																																		
33	Alpha Lock Indicator	ALI	ALI will indicate if op code XX101 is selected. (See operation codes). In the standard device there is no other function. If alpha lock is selected as an option, op code XX101 will result in bit 6 being replaced by bit 9 when a key is depressed.																																		
34	Shift Lock Indicator	SLI	SLI will indicate if op code XX011 is selected (see operation codes). In the standard device this op code will also select the shift lock function.																																		
35	Key Pressed	\overline{KPD}	\overline{KPD} is used to shift the threshold of the external sense amplifier in order to provide hysteresis to improve noise immunity. In addition \overline{KPD} may be inverted to provide the data input to the 8 bit latches for decoding X14 and X15. When a key closure is detected \overline{KPD} is generated causing the 8 bit latch output to go high. See figure 2.																																		
36	CLOCK	CLK	Resistor/capacitor tie point for the internal oscillator. Nominal frequencies and scan times are shown below:																																		
<table><tr><th rowspan="2">R</th><th colspan="2">C = 150pf</th><th colspan="2">C = 220pf</th><th colspan="2">C = 500pf</th></tr><tr><th>Freq</th><th>Scan time</th><th>Freq</th><th>Scan time</th><th>Freq</th><th>Scan time</th></tr><tr><td>5K</td><td>1 3 MHz</td><td>1 5 msec</td><td>1 2 MHz</td><td>1 7 msec</td><td>71 MHz</td><td>2 8 msec</td></tr><tr><td>10K</td><td>8 MHz</td><td>2 3 msec</td><td>.8 MHz</td><td>2 7 msec</td><td>45 MHz</td><td>4 3 msec</td></tr><tr><td>25K</td><td>4 MHz</td><td>4 8 msec</td><td>3 MHz</td><td>6 0 msec</td><td>20 MHz</td><td>10 0 msec</td></tr></table>				R	C = 150pf		C = 220pf		C = 500pf		Freq	Scan time	Freq	Scan time	Freq	Scan time	5K	1 3 MHz	1 5 msec	1 2 MHz	1 7 msec	71 MHz	2 8 msec	10K	8 MHz	2 3 msec	.8 MHz	2 7 msec	45 MHz	4 3 msec	25K	4 MHz	4 8 msec	3 MHz	6 0 msec	20 MHz	10 0 msec
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5K	1 3 MHz	1 5 msec	1 2 MHz	1 7 msec	71 MHz	2 8 msec																															
10K	8 MHz	2 3 msec	.8 MHz	2 7 msec	45 MHz	4 3 msec																															
25K	4 MHz	4 8 msec	3 MHz	6 0 msec	20 MHz	10 0 msec																															
37	Reset	\overline{POR}	Reset clears all internal registers and flip flops. Suggested circuit for power on reset is illustrated in Figure 1.																																		
38	Matrix Input	\overline{MATIN}	Input from external multiplexer. Senses signal from X-Y scan of depressed key.																																		
39	Any Key Down Strobe	AKD	AKD is low when no key is depressed. When a key is depressed AKD goes high. If, while one key is held, a second key is depressed, AKD will go low for 2 clock cycles.																																		
40	Power	V _{CC}	Power supply +5V input																																		

OPERATION

Keys are connected in a 16 x 8 matrix. Scanning of the matrix is performed by the encoder in conjunction with an external, multiplexer. The encoder provides a 3 bit binary address (YA, YB, YC) used to scan each of eight possible sense lines (Y-lines). The drive lines (X-lines) are each pulsed low by the encoder. If a key is closed, the pulse is coupled from the drive to the sense lines, amplified, and sent to the encoder. When used to encode reactive switches, a detection circuit is necessary between the output of the multiplexer and the $\overline{\text{MATIN}}$ input to the encoder. In this manner, each matrix cross-point is interrogated in turn. Each matrix cross-point is given a unique binary code that is determined by the internal scan counters. This code is used to address a ROM which generates the output codes (such as ASCII or other customer defined codes). The output of the ROM is entered into an output holding register when the key is determined to be a valid key closure. Only the cross-points on X0 through X13 can have output codes: X14 and X15 can be used for scanning discrete keys.

An internal oscillator controls the matrix scanning rate. The minimum scanning time is 1.7 ms, at a 1.2 MHz clock. This allows a burst typing speed equivalent to over 250 words/min. When a key is depressed, a matrix address from an X driver and Y input line representing that key is loaded into a 7 bit latch. On the second keyboard scan, the matrix address and the stored address are compared. If the two addresses match, the ROM 10 bit word at that address is loaded into the data holding register. This data remains valid until the next key is depressed. The internal error flag is set, if this option was utilized, whenever there is a mismatch between 7 bit addresses.

Two negative pulses must be detected during the $\overline{\text{MATIN}}$ timing window for the depression to be recognized.

Keyboard Selection

The AY-3-4592 keyboard encoder can be used with a wide variety of available keyboards. An external multiplexing circuit and one external sense amplifier can be tailored to the user's specific requirements. As shown in Figure 1, the sense amplifier detects changes in voltage caused by variations in the switch impedance as a key is depressed and released. Given the key switch impedances for depressed and released states, the values of Rx and Rh can be chosen to guarantee switch closure detection and noise margins. Rx is chosen to match the capacitor or reactor time constants. For example, given a variable capacitance keyboard switch with C1 = 100pf, and C2 = 10pf for depressed and released positions respectively, with a 1.5MHz oscillator and Rx = 10 Kohm, a depressed key would make a 4.7 volt pulse while a raised key would produce a 2.6 volt pulse. The potentiometer would then be set for best noise immunity with minimum pulse

width, 90ns for all keys. The hysteresis resistor, Rh, is chosen at roughly ten times the value of Rx to provide increased noise immunity for detected key depressions.

Operation Codes

Depending on the internal programming of the AY-3-4592, keys may have one of three different functions. Keys on matrix line X0 through X13 have, in addition to the output code bits, a function flag bit (FFB). If the FFB is programmed as a zero, the key produces a data output when depressed.

When FFB is a one, the key is a "function" key for which bits 1-5 determine the function. These bits are referred to as the op code and are used to provide special functions such as shift, shift lock, alpha lock, etc. Bits 6-10 are not used.

Op codes may be programmed to provide data outputs as well as change the mode of operation. Data when outputted is not latched as are normal coded outputs.

Bits 1-3 indicate what operation the key will perform; per table 1.

Bit 4 programmed as one indicates a down-coded key, for which the 10 data bits programmed in the shift mode level of ROM are outputted when the key is depressed.

Bit 5 programmed as one indicates an up-coded key for which the 10 data bits programmed in the control mode level of ROM are outputted when the key is released.

Neither bit 4 nor 5 will have any effect on the operational control of bits 10-3.

Table 1

Op-Code					Function
5	4	3	2	1	
X	X	0	0	0	Function key (with up/down codes)*
X	X	0	0	1	Right Shift Key
X	X	0	1	0	Left Shift Key
X	X	0	1	1	Shift Lock Key or Discrete Key (output SLI)
X	X	1	0	0	Control Key
X	X	1	0	1	Alpha Lock Key or Discrete Key (output ALI)
X	0	1	1	0	Error Reset Key or discrete key (output X15)
X	X	1	1	1	Discrete Key (output D10)

*If the op-code is 00000 the key has no internal function but $\overline{\text{KPD}}$ will go low when it is processed.

OPTIONS

Pin or Function	Option
X15	<p>X15 may be programed as</p> <ol style="list-style-type: none"> 1) an X-output to provide a second set of 8 discrete lines 2) a discrete output which indicates when a function key with op code XX110 is depressed 3) an Error Flag Indicator (EFI). See Error Flag <p>In the AY-3-4592 STD X15 is a discrete output</p>
Error Flag	<p>When this option is selected, the AY-3-4592 has the capability of detecting multiple key depressions during the same scan cycle. When selected, the error flag may be programed to generate KBINH and or appear at the X15 output. The error flag may be reset by three methods. If the automatic reset is selected/the flag will be reset when the error causing Key is released.</p> <p>Op-code XX110 may be programed on a function key to reset the error flag.</p> <p>If pin 12 is programed for KBINH error flag will be reset by pulsing pin 12 high. The reset will occur on the negative edge of the KBINH signal; the pulse must be at least 16 clock cycles.</p> <p>Error flag causes KBINH and is automatically reset.</p>
Alpha Lock	<p>When programed for Alpha lock, the function key with op-code XX101 will cause the bit 6 output to be replaced by bit 9. Bit 9 is not altered. Alpha lock is normally used to force printing of upper case characters irrespective of the shift function. Op Code XX101 will also cause an output on ALI (pin 33).</p> <p>When Alpha lock is not programed, op code XX101 will result in an output on ALI (pin 33).</p> <p>Op code XX101 may be programed for momentary action, or latched push-on, push-off alternating action. ALI may be programed for normally low or high output.</p> <p>Op code XX101 is momentary action. ALI is normally low.</p> <p>The AY-3-4592 STD is not programed for Alpha lock, although there will be an output on ALI.</p>
Shift Lock	<p>When programed for shift lock, the function key with op-code XX011 will cause normal electronic shift action. Op code XX011 will also cause an output on SLI (pin 34).</p> <p>If shift lock is not programed, op code XX011 will simply cause an output on SLI. SLI may be programed for normally low or high output.</p> <p>The AY-3-4592 STD is programed for shift lock operation with SLI normally low.</p>
KBINH	<p>KBINH, Keyboard Inhibit, may be programed to be caused by Pin 12 high, by the error flag, or both. In addition, function keys with up or down codes may be programed, as a group, to be inhibited by KBINH. This is the KCI Out option.</p> <p>When pin 12 is programed to cause KBINH, a high input on pin 12 will inhibit processing of common keys.</p> <p>If a key is depressed while the KBINH signal is present, output and output strobe will be generated when KBINH is released.</p> <p>The AY-3-4592 STD has KBINH actuated by pin 12 high, and by the error flag. The KCI In option is used, that is, the function key operation is independent of KBINH.</p>
D10	<p>D10, pin 11, may be programed as the output for the memory bit 10 or as a discrete output. As a discrete output, pin 10 is switched from its normal state (programmable as high or low) by the function key with op-code XX111.</p> <p>The AY-3-4592 STD is programed for D10 as a discrete key, normally low.</p>
Key Type	<p>Keys may be either normally open or normally closed. The AY-3-4592 STD is designed for normally open keys.</p>

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{CC} -0.3 Volts to +7.0 Volts
 Maximum voltage with respect to V_{CC} +0.3 Volts
 Storage Temperature 65°C to +150°C
 Operating Temperature 0 to 70°C

Standard Conditions (unless otherwise noted)

$V_{CC} = 5.0V \pm 5\%$

$T_A = 0^\circ$ to 70°C

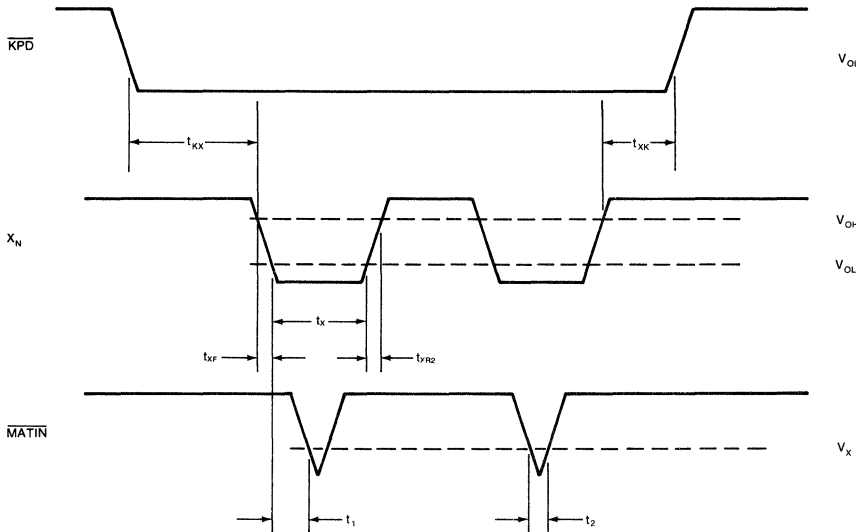
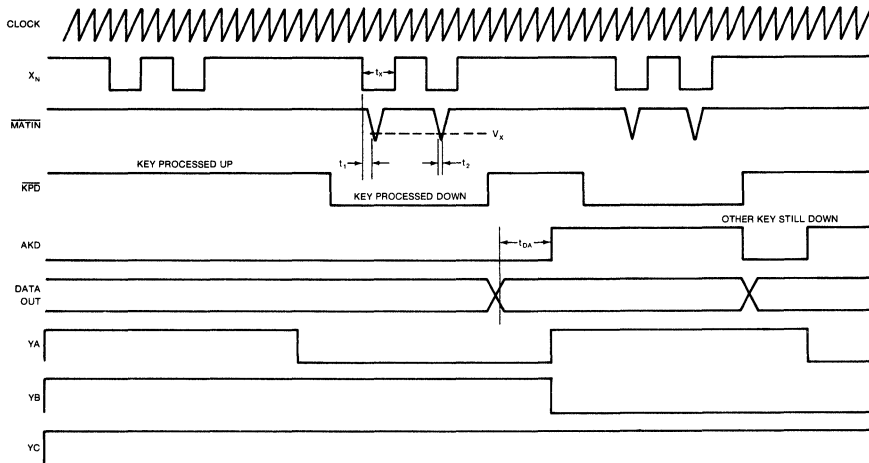
* Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

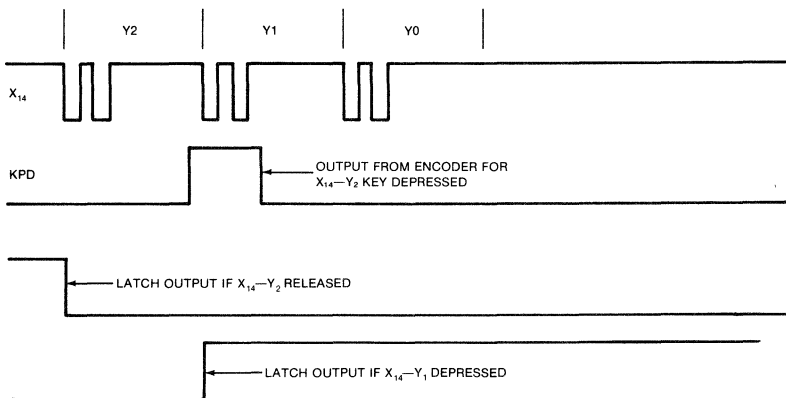
Characteristic	Symbol	Min.	Typ.**	Max.	Unit	Condition
Data Output "1" Voltage	V_{OH}	3.5	-	-	V	$I_{OH} = 50\mu A$, 25pf
Data Output "0" Voltage	V_{OL}	-	-	0.5	V	$I_{OL} = 1.6mA$
All Inputs "1" Voltage	V_{IH}	2.2	-	-	V	except \overline{POR} , 2KRO
All Inputs "0" Voltage	V_{IL}	-	-	0.8	V	except \overline{POR} , 2KRO
All Inputs Leakage	I_{IH}	-	-	10	μA	$V_{in} = 5V$
X Output "1" Voltage	X_{OH}	3.5	-	-	V	$I_{OH} = 50\mu A$, 100pf
X Output "0" Voltage	X_{OL}	-	-	0.5	V	$I_{OL} = 1.6mA$
AKd Output Voltage	V_A	-	-	0.6	V	$I_{OL} = 3.2mA$
MATIN Input Voltage	V_X	-	-	0.4	V	
\overline{POR} , 2KRO high threshold	V_{SH}	-	1.3	-	V	Schmitt trigger
\overline{POR} , 2KRO low threshold	V_{SL}	-	3.7	-	V	Schmitt trigger
Power Supply Current	I_{CC}	-	35	60	mA	$V_{CC} = 5.3V$
Clock Frequency	ϕ	200	-	1200	kHz	
Matrix Delay	t_1	-	-	250	ns	
Input pulse width	t_2	90	-	-	ns	
X Output pulse width	t_x	1.7	-	-	μs	
X Output fall time	t_{XF}	-	-	150	ns	$V_{OH} = 4.3V$, $V_{OL} = 0.4V$
X Output rise time	t_{XR1}	-	-	150	ns	$V_{OH} = 2.4V$, $V_{OL} = 0.4V$
X Output rise time	t_{XR2}	-	-	500	ns	$V_{OH} = 3.5V$, $V_{OL} = 0.4V$
X Output rise time	t_{XR3}	-	-	1500	ns	$V_{OH} = 4.3V$, $V_{OL} = 0.4V$
\overline{KPD} -X Output set time	T_{KX}	500	-	-	ns	
X Output- \overline{KPD} hold time	t_{XK}	100	-	-	ns	
Data out to AKD time	t_{OA}	1.7	-	-	μs	

**Typical values are at +25°C and nominal voltages.

TIMING DIAGRAMS



Discrete Function Key



READ ONLY MEMORY

CODE CHART / AY-3-4592-STD

XXY	F	-----NORMAL-----		-----SHIFT-----		-----CONTROL-----		--SHIFT/CONTROL--	
		HEX	BINARY	HEX	BINARY	HEX	BINARY	HEX	BINARY
000	1	001	000000001	Right Shift	3FF	111111111		3FF	111111111
001	1	002	000000010	Left Shift	3FF	111111111		3FF	111111111
002	1	003	000000011	Shift Lock	3FF	111111111		3FF	111111111
003	1	004	000000100	Control	3FF	111111111		3FF	111111111
004	1	005	000000101	AL1	3FF	111111111		3FF	111111111
005	1	006	000000110	X15	3FF	111111111		3FF	111111111
006	1	007	000000111	D10	3FF	111111111		3FF	111111111
007	0	00E	001100110	1	00E	001100110	1	00E	001100110
010	0	1E4	011110010	ESC	1E4	011110010	ESC	1E4	011110010
011	0	0CD	001100110	2	1BF	011011111	@	0CD	001100110
012	0	0CD	001100110	2	0DD	001101101	"	0CD	001100110
013	0	1A8	011001000	W	1A8	011010100	W	1E8	011110100
014	0	1BE	011001110	9	1AE	011101110	Q	1EE	011110110
015	0	1BC	011001100	S	1AC	011010100	S	1EC	011110100
016	0	19E	011011110	a	1BE	011111110	A	1FE	011111110
017	0	185	011000101	Z	1A5	011010010	Z	1E5	011110010
020	0	17F	010111111	NUL	17F	010111111	NUL	17F	010111111
021	0	0CB	001100101	4	0DB	001101011	\$	0CB	001100101
022	0	0CC	001101100	3	0DC	001101100	#	0CC	001101100
023	0	180	011000101	r	1A0	011010101	R	1ED	011110101
024	0	19A	011001010	e	18A	011011010	E	1FA	011111010
025	0	198	011001011	d	188	011011011	D	1F9	011111011
026	0	187	011000011	x	1A7	011010011	X	1E7	011110011
027	0	19C	011001100	c	18C	011011100	C	1FC	011111100
030	0	17E	010111110	SOH	17E	010111110	SOH	17E	010111110
031	0	17D	010111101	STX	17D	010111101	STX	17D	010111101
032	0	0CA	001100101	5	0DA	001101010	%	0CA	001100101
033	0	18B	011001011	t	1AB	011010101	T	1EB	011110101
034	0	199	011001001	f	189	011011001	F	1F9	011111001
035	0	198	011001000	g	188	011011000	G	1F8	011111000
036	0	189	011000101	v	1A9	011010101	V	1E9	011110101
037	0	19D	011001101	b	1BD	011011101	B	1FD	011111101
040	0	17C	010111100	ETX	17C	010111100	ETX	17C	010111100
041	0	0CD	001100100	7	0D9	001101001	7	0C8	001100100
042	0	0C9	001100101	6	0D9	001101001	6	0C9	001100101
043	0	186	011000010	y	1A6	011010010	Y	1E6	011110010
044	0	197	011001011	h	187	011010111	H	1F7	011110111
045	0	191	011001001	n	181	011010001	N	1F1	011110001
046	0	0C9	001100101	6	0C3	001100001	<	0C9	001100001
047	0	0DF	001101111	SP	0DF	001101111	SP	0DF	001101111
050	0	178	010111011	EOT	178	010111011	EOT	178	010111011
051	0	0C7	001100011	8	0D5	001101011	*	0C7	001100011
052	0	0C8	001100100	7	0D8	001101000	7	0D8	001100100
053	0	18A	011000101	u	1AA	011010101	U	1EA	011110101
054	0	195	011001010	J	185	011011010	J	1F5	011111010
055	0	194	011001000	k	184	011011000	K	1F4	011111000
056	0	1A2	011001001	m	182	011111001	M	1F2	011111001
057	0	0D3	001100011	<	0C3	001100001	<	0D3	001100011
060	0	17A	010111101	ENQ	17A	010111101	ENQ	17A	010111101
061	0	0C6	001100010	9	0D7	001100011	(0C6	001100010
062	0	0C7	001100011	8	0D7	001100011	(0C7	001100011
063	0	1A6	011001010	I	186	011010110	I	1F6	011110110
064	0	190	011001000	O	180	011010000	O	1F0	011110000
065	0	194	011001001	K	1A4	011010010	K	1F4	011110010
066	0	193	011001001	L	183	011010011	L	1F3	011110011
067	0	192	011001001	M	1A2	011010010	M	1F2	011110010
070	0	179	010111101	ACK	179	010111101	ACK	179	010111101
071	0	0CF	001100111	#	0D6	001100111	#	0CF	001100111
072	0	0C6	001100010	9	0D6	001100010	9	0C6	001100010
073	0	178	010111100	BEL	178	010111100	BEL	178	010111100

CODE CHART / AY-3-4592-STD

XXY	F B	-----NORMAL-----			-----SHIFT-----			-----CONTROL-----			--SHIFT/CONTROL--	
		HEX	BINARY		HEX	BINARY		HEX	BINARY		HEX	BINARY
074	0	18F	0110001111	P	1AF	0110101111	P	1EF	0111101111	DLE	1EF	0111101111 DLE
075	0	0C4	0011000100	:	0C5	0011000100	:	0C4	0011000100	:	0C5	0011000101 :
076	0	193	0110010011	L	1A3	0110100011	\	1F3	0111110011	FF	1E3	0111100011 FS
077	0	001	0011010501	.	0C1	0011000001	>	001	0011010001	-	0C1	0011000001 >
080	0	092	0011010100	-	1A0	0110100000	(002	0011010010	-	1A0	0110100000 -
081	0	021	0110010001	n	1A1	0110100001)	1F1	0111110001	SI	1E1	0111100001 RS
082	0	18F	0110001111	P	18F	0110111111	@	1EF	0111101111	DLE	1FF	0111111111 NUL
083	0	1A4	0110100100		1A2	0110100010]	1E4	0111100100	ESC	1E2	0111100010 " GS
084	0	008	0011011000	'	00D	0011011101	~	008	0011011000	'	00D	0011011101 +
085	0	0C4	0011000100	/	004	0011010100	+	0C4	0011000100	/	004	0011010100 ?
086	0	00D	0011011000	/	0C0	0011000000	+	00D	0011010000	/	0C0	0011000000 =
087	0	177	0101110111	BS	177	0101110111	BS	177	0101110111	BS	177	0101110111 BS
090	0	0C2	0011000010	=	004	0011010100	+	0C2	0011000010	=	004	0011010100 *
091	0	0C5	0011000101	=	005	0011010101	*	0C5	0011000101	=	005	0011010101 *
092	0	176	0101110110	HT	176	0101110110	HT	176	0101110110	HT	176	0101110110 HT
093	0	1A3	0110100011	\	083	0010000011	'	1E3	0111100011	FS	1E3	0111100011 FS
094	0	175	0101110101	LF	175	0101110101	LF	175	0101110101	LF	175	0101110101 LF
095	0	1A4	0110100100		084	0010000100		1E4	0111100100	ESC	1E4	0111100100 ESC
096	0	1F2	0111110010	CR	1F2	0111110010	CR	1F2	0111110010	CR	1F2	0111110010 CR
097	0	1A2	0110100010] DEL	082	0010000010] DEL	1E2	0111100010	GS	1E2	0111100010 GS
100	0	080	0010000000	DEL	080	0010000000	DEL	080	0010000000	DEL	080	0010000000 DEL
101	0	174	0101110100	VT	174	0101110100	VT	174	0101110100	VT	174	0101110100 VT
102	0	002	0011010010	-	1A0	0110100000	-	1E0	0111100000	US	1E0	0111100000 US
103	0	173	0101110011	FS	173	0101110011	FS	173	0101110011	FS	173	0101110011 FS
104	0	1F5	0111110101	LF	1F5	0111110101	LF	1F5	0111110101	LF	1F5	0111110101 LF
105	0	18F	0110111111	@	1A3	0110100011	~	1FF	0111111111	NUL	1FF	0111111111 NUL
106	0	1A1	0110100001	~	081	0010000001	~	1E1	0111100001	RS	1E1	0111100001 RS
107	0	1A0	0110100000	-	072	0011000010	-	1A0	0110100000	-	0C2	0011000010 =
110	0	172	0101110010	CR	172	0101110010	CR	172	0101110010	CR	172	0101110010 CR
111	0	1F6	0111110110	HT	1F6	0111110110	HT	1F6	0111110110	HT	1F6	0111110110 HT
112	0	002	0011010010	-	0C2	0011000010	=	002	0011010010	-	0C2	0011000010 =
113	0	171	0101110001	SO	171	0101110001	SO	171	0101110001	SO	171	0101110001 SO
114	0	190	0110010000	o	1A0	0110100000	o	1F0	0111100000	SI	1E0	0111100000 SI
115	0	1A4	0110100100		1A2	0110100010		1A4	0110100100		1A2	0110100010
116	0	1F7	0111110111	BS	1F7	0111110111	BS	1F7	0111110111	BS	1F7	0111110111 BS
117	0	1A0	0110100000	US	1A0	0110100000	US	1A0	0110100000	US	1A0	0110100000 US
120	0	170	0101110000	SI	170	0101110000	SI	170	0101110000	SI	170	0101110000 SI
121	0	0C8	0011001000	7	0C8	0011001000	7	0C8	0011001000	7	0C8	0011001000 7
122	0	1F4	0111110100	VT	1F4	0111110100	VT	1F4	0111110100	VT	1F4	0111110100 VT
123	0	1A6	0101110111	DLE	1A6	0101110111	DLE	1A6	0101110111	DLE	1A6	0101110111 DLE
124	0	0C8	0011001011	4	0C8	0011001011	4	0C8	0011001011	4	0C8	0011001011 4
125	0	003	0011010011	.	003	0011010011	.	008	0011010011	.	003	0011010011 .
126	0	0CE	0011001110	i	0CE	0011001110	i	0CE	0011001110	i	0CE	0011001110 i
127	0	0CF	0011001111	ø	0CF	0011001111	ø	0CF	0011001111	ø	0CF	0011001111 ø
130	0	1A6	0101110110	DC1	1A6	0101110110	DC1	1A6	0101110110	DC1	1A6	0101110110 DC1
131	0	0C6	0011000110	9	0C6	0011000110	9	0C6	0011000110	9	0C6	0011000110 9
132	0	0C7	0011000111	8	0C7	0011000111	8	0C7	0011000111	8	0C7	0011000111 8
133	0	0CA	0011001010	5	0CA	0011001010	5	0CA	0011001010	5	0CA	0011001010 5
134	0	0C9	0011001001	6	0C9	0011001001	6	0C9	0011001001	6	0C9	0011001001 6
135	0	0CD	0011001101	2	0CD	0011001101	2	0CD	0011001101	2	0CD	0011001101 2
136	0	0CC	0011001100	3	0CC	0011001100	3	0CC	0011001100	3	0CC	0011001100 3
137	0	001	0011010001		001	0011010001		001	0011010001		001	0011010001

OPTIONS ARE

Error Flag — Programmed
 X15 — Discrete output, normally low
 KBINH — Set by high on pin 12 or error flag Function keys not inhibited by KBINH
 Error Flag — Reset by releasing error-causing key
 Shift Lock — Operational SLI normally low
 Alpha Lock — Inhibited ALI normally low, set by OP code XX101
 D10 — Discrete output, normally low
 Key Type — Normally open

NOTE Bit 9 — Programmed to allow alpha lock implementation using external logic
 Bit 8 — Programmed low for "mono mode" keys, for which the output is the same in all modes
 Bits 1-7 — "Inverted" ASCII data bits

AY-3-4592

GENERAL
INSTRUMENT

READ ONLY MEMORY

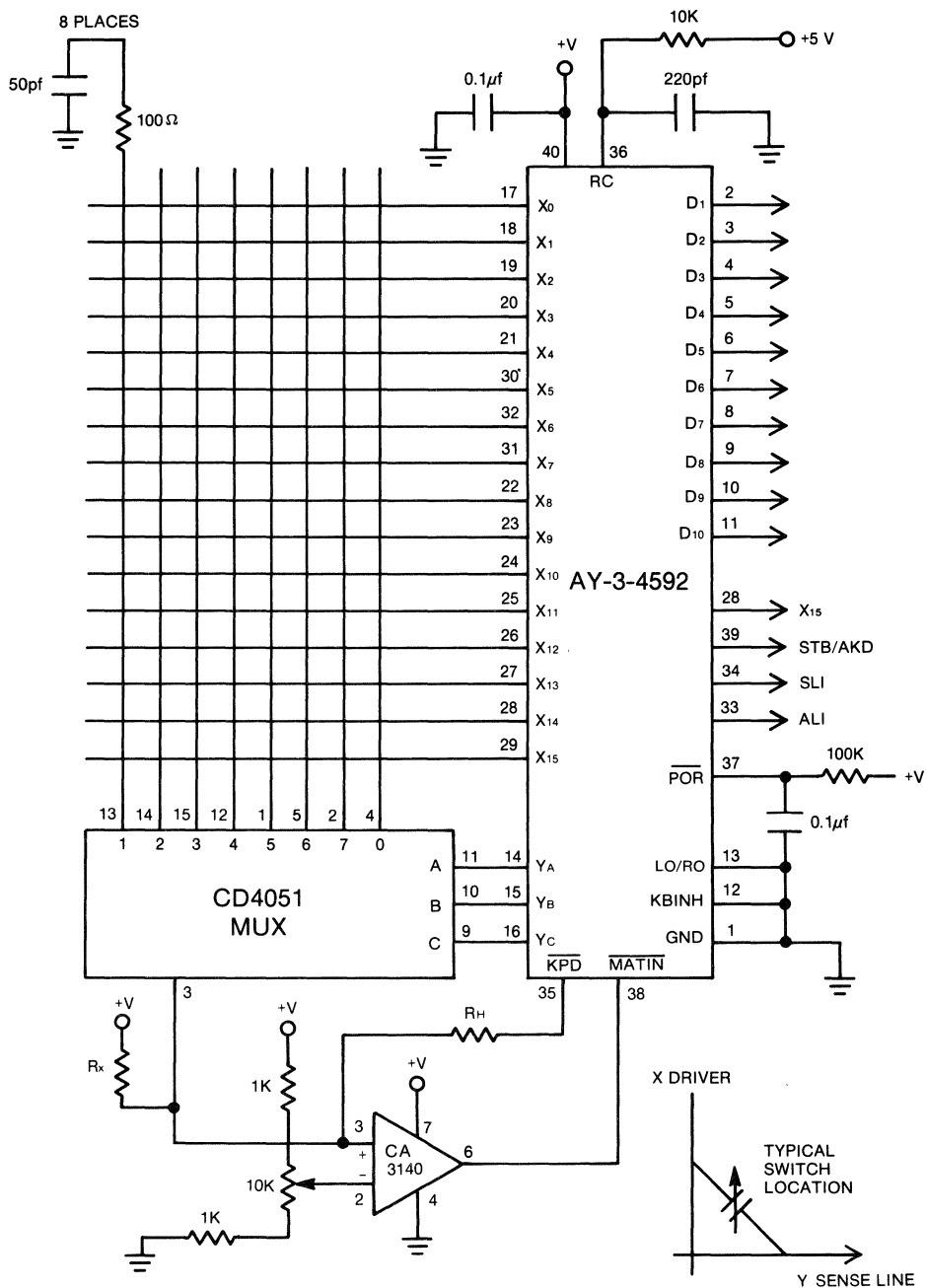


Fig. 1 SAMPLE KEYBOARD DESIGN ROM CODED KEYS

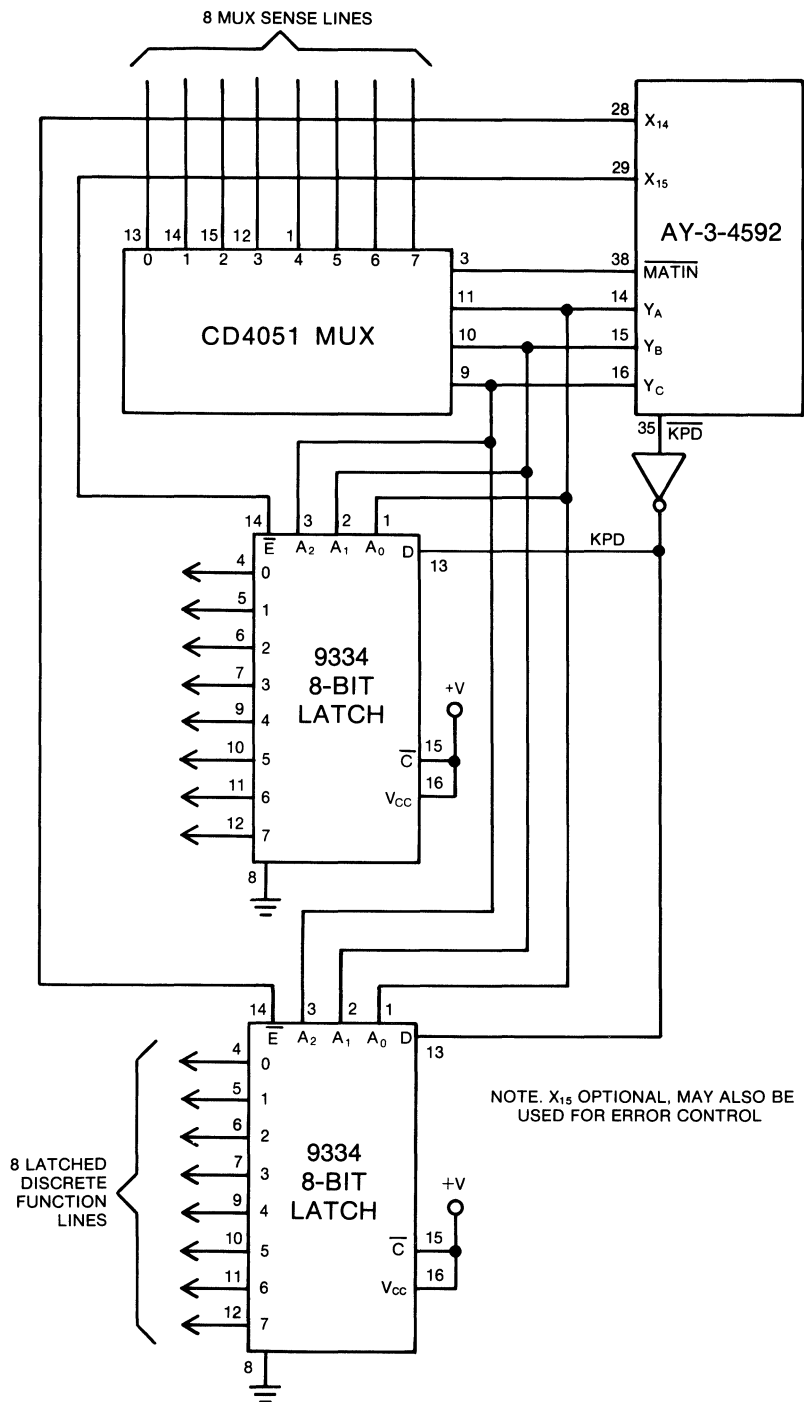


Fig. 2 SAMPLE KEYBOARD DESIGN DISCRETE FUNCTION KEYS