

Keyboard Encoder Read Only Memory KEM

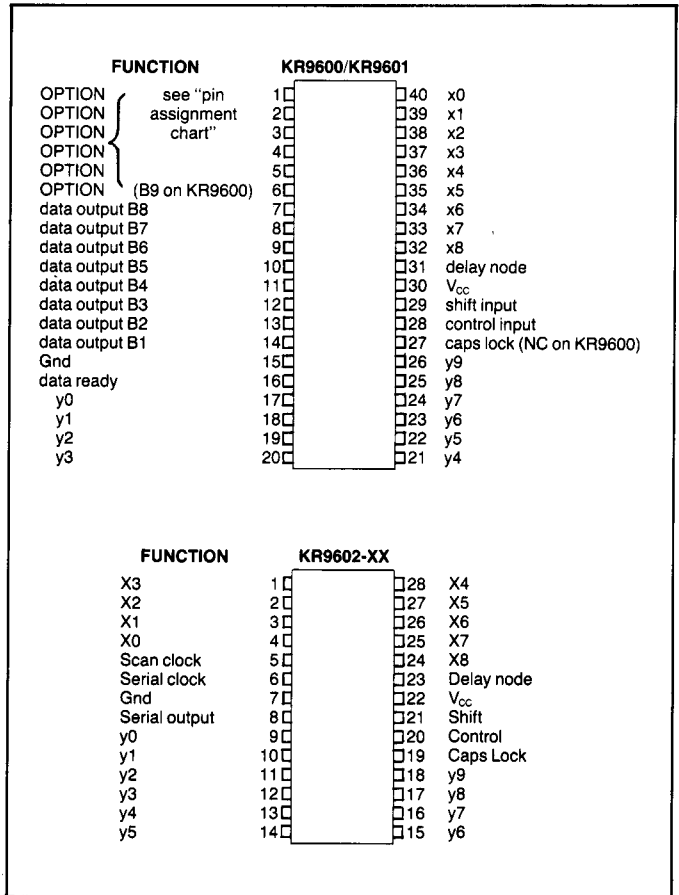
FEATURES

- On-chip "caps" lock (KR9601, KR9602)
- On-chip auto repeat (KR9601, KR9602)
- Contact bounce protection
- N Key Rollover or Lockout operation
- Hysteresis on keyboard matrix inputs
- Tri-state TTL compatible data outputs
- Serial output (on KR9602 only)
- Quad Mode (Normal, shift, control, shift-control)
- High frequency clock input
- Pin-compatible with KR3600 (KR9600)
- Static charge protection on all inputs and outputs
- + 5 volt supply

EXTERNALLY SELECTABLE OPTIONS ON KR9600 AND KR9601

- Pulse or level data ready output signal
- External clock input
- On chip master/slave oscillator
- All 10 output bits available
- Lockout/Rollover external selection
- Chip enable external selection
- Data complement control
- Any Key Down output
- Selectable Auto-Repeat rate
- Programmable Auto-Repeat rate

PIN CONFIGURATION*



*PLCC (J LEAD QUAD PACK) also available.

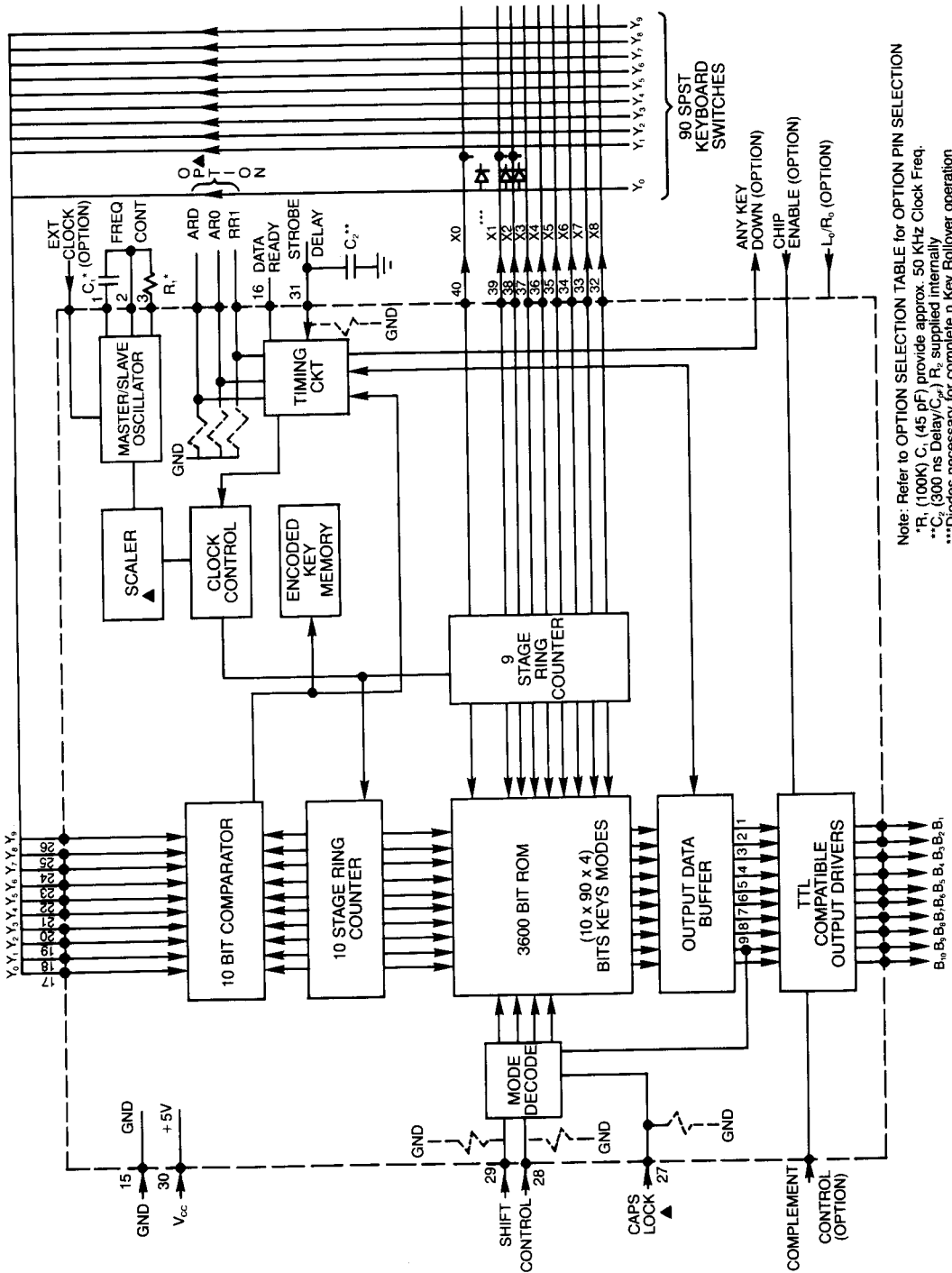
GENERAL DESCRIPTION

The KR9600/1/2 is a keyboard encoder that contains all the logic necessary to debounce and encode SPST key-switches into a fully decoded data output of up to 10 bits. The KR9600/1/2 contains a 3600 bit ROM, 9 stage and 10 stage ring counters, a 10 bit comparator, timing circuitry, a 90 bit memory to store the location of encoded keys for N key rollover operation, an externally controllable delay net-

work for eliminating the effect of contact bounce, an output data buffer and TTL compatible output drivers.

The KR9600 and the KR9601 provide a parallel data output in a 40 pin configuration with pin selectable options, while the KR9602 provides a serial asynchronous output in a 28 pin configuration with mask programmable options. (Ref. KR9600/1/2 custom coding information sheet).

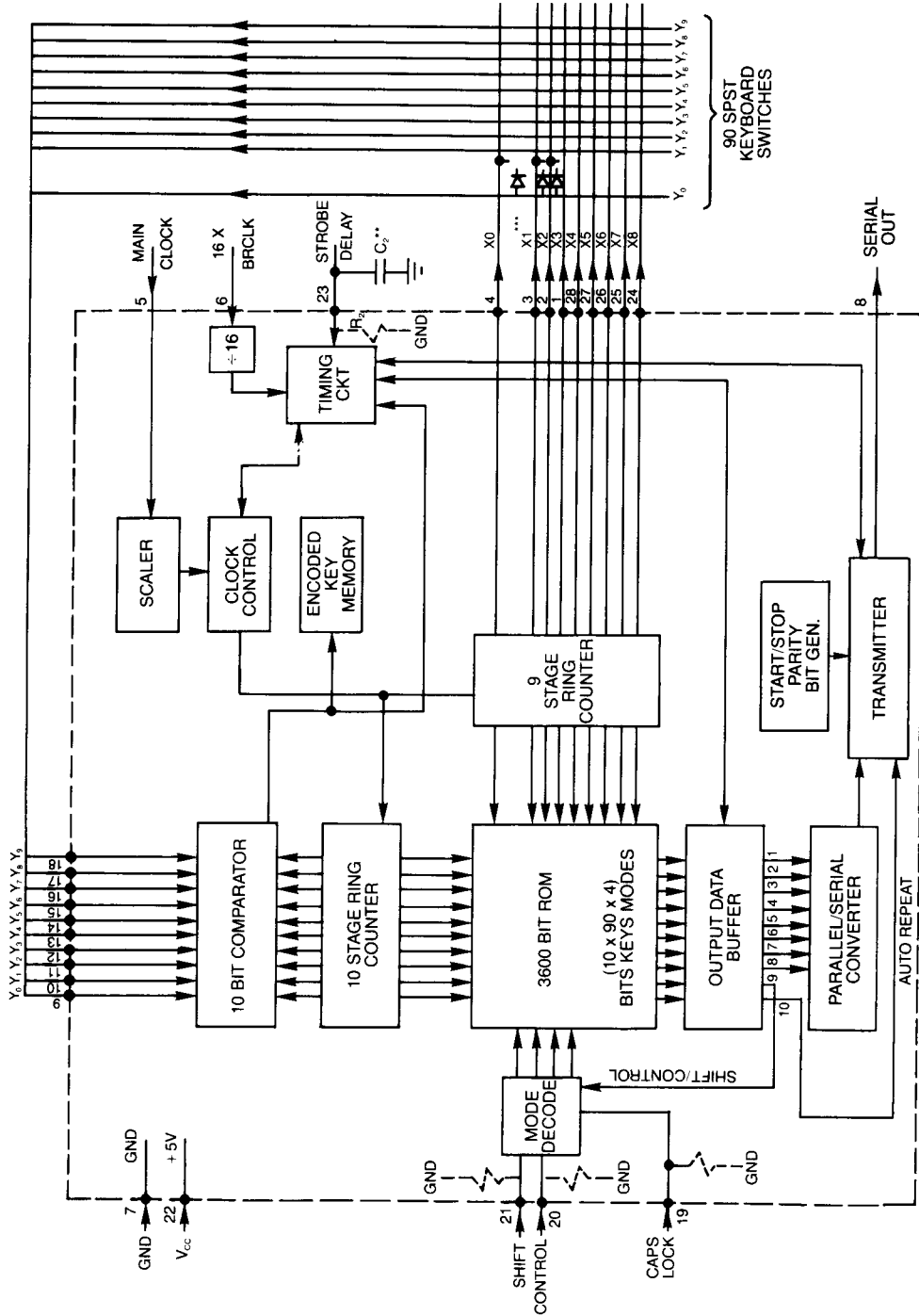
BLOCK DIAGRAM FOR KR9600/KR9601



Note: Refer to OPTION SELECTION TABLE for OPTION PIN SELECTION
 *R₁ (100K) C₁ (45 pF) provide approx. 50 KHz Clock Freq.
 **C₂ (300 ns Delay/C₂) R₂ supplied internally
 ***Diodes necessary for complete n Key Rollover operation

▲ Not Available on KR9600

BLOCK DIAGRAM FOR THE KR9602



Note: **C₂ (300 ns Delay/C₂) F₂ supplied internally
 ***Diodes necessary for complete n Key Rollover operation

DESCRIPTION OF PIN FUNCTIONS

NAME	SYMBOL	KR9600 PIN #	KR9601 PIN #	KR9602 PIN #	FUNCTION
X OUTPUTS	X0-X8	40-32	40-32	4-1 28-24	External outputs from the 9-stage ring counter to the keyboard to form X-Y matrix with the keyboard switches as the crosspoints.
Y INPUTS	Y0-Y9	17-26	17-26	9-18	External inputs from the keyboard X-Y matrix.
EXTERNAL CLOCK (see note)	***	1	1	5	External clock input.
SERIAL CLOCK	***	***	***	6	Serial input Baud rate clock, for KR9602.
DATA OUTPUTS	B8-B1	7-14	7-14	8	Data outputs B1-B8. Parallel outputs for the KR9600/9601, serial output for the KR9602.
DATA READY	DR	16	16	N/A	This output, which can be a level or a pulse, signals that a key closure has been detected and that data is available at the output port.
DELAY NODE INPUT	DELAY	31	31	23	Externally controllable delay network for eliminating the effect of switch contact bounce.
SHIFT INPUT	SHIFT	29	29	21	This input is used to select the shift mode data.
CONTROL INPUT	CNTRL	28	28	20	This input is used to select the control mode data. Simultaneous assertion of shift and control inputs will place the encoder into the shift-control mode.
CAPS LOCK	CAPS	see note	27	19	This input "ANDed" with bit B9 of the ROM will cause a mode shift. See "programming options".
POWER SUPPLY	V _{cc}	30	30	22	+ 5V power supply.
GROUND	Gnd	15	15	7	Ground.
OPTION PINS		see note	1-6	N/A	See option selection table for pin assignment.

Note: Caps Lock and Auto-Repeat are not available on KR9600.
See option selection table for pin assignment.

DESCRIPTION OF OPERATION

The main clocks for the KR9600 and KR9601 are derived from either an external clock source or the internal oscillator. The KR9602 requires an external clock. The external clock is routed to a divider with a mask programmable division rate from 1 to 63 to generate the internal clock.

The keys are scanned in a nine output by ten input matrix, each key having a unique input-output combination connected to it. The inputs all go selectively to a level detector which has logically variable (1's and 0's) levels and hysteresis. The outputs are enabled one at a time from output X0 towards X8, at a rate of 10-100KHz, through a 9 stage ring counter. The 10 inputs are searched one at a time from Y0 to Y9, through a 10 stage ring counter, each time one of the outputs is enabled. The output and input pins all have pullups to V_{cc} and are precharged each clock even if the scan is stopped at one key. When a level on the selected path to the comparator matches a level on the corresponding comparator input from the 10 stage ring counter and the key has not been encoded, the switch bounce delay network is enabled. The key down stroke is examined, without advance to the next key location, until the key has been stable for the length of the DELAY CAP pin to discharge. The code for the depressed key is transferred to the output data buffer and the data ready signal appears.

The scan has two modes as determined by the L0ckout/Rollover option. Once a key is determined to be down the scan will not advance if in the L0ckout mode. Consequently a new key closure is not detected until the previously depressed key is released. The scan sequence will resume upon key release and the output data buffer stores the code of the last key encoded. In the Rollover mode a "1" is stored in the encoded key memory and the scan sequence is resumed and the code for the last encoded key remains in the data output buffer. Each depressed key is encoded regardless of the state of the previously depressed keys. The internal keyboard ROM is 10 bits wide. Bits 1-8 are output via data outputs B1-B8. Bits 9 and 10 may be output as data and/or utilized respectively for Caps-lock and Auto-repeat select. This allows mask programmable selection of which keys will have caps-lock and auto-repeat. When selected, the auto repeat will commence with a "long" delay after key depression followed by "short" delays. The duration of the delays varying with the clock frequency and the state of the ARD, AR0, and AR1 signals.

A Chip Enable input is available to enable the parallel output buffer. Data Ready can be put in the high-impedance state with Chip Enable (CE) or can be open drain as a mask programmable option to facilitate wire-oring as an interrupt.

In the serial output version of KR9602, when a key is debounced and then called valid, the serial shift register is loaded with the data (8 bits B1-B8) from the ROM, the data from the parity generator, and the data from the start and stop bits generator. Bits B9 and B10 are internally used respectively for Caps-lock and Auto-repeat select. The data register is then allowed to shift data out at the rate of one bit per 16 clocks of the baud rate clock pin, on the negative edge of that clock. If the baud rate clock is too slow with respect to the internal clock, and the keyboard were allowed to continue scanning when the data register is loaded, then new data could be loaded on top of shifting-out data.

To avoid this, if a new key is depressed before the previous data is fully shifted out of the device, including the stop bits, the delay cap will be allowed to decay but the internal logic will delay its effect until the shift out of the previous data is completed. If the new key is released before the end of the extended delay time it will not be encoded.

OPTION SELECTION TABLE

Since the selected coding of each key and all the options are defined during the manufacture of the chip, the coding and options can be changed to fit any particular application of the keyboard. Up to 360 codes of up to ten bits can be programmed into the KR9600/KR9601 ROM covering most popular codes such as ASCII, EBCDIC, SELECTRIC etc. as well as many specialized codes.*

Pin Assignment for KR9600/KR9601

The chip pins from pin #1 thru pin #6 are optionally connected to differing logic functions. Many of the functions are available on more than one pin.

PROGRAMMING OPTIONS

The various options on the KR9600 and KR9601 are user selectable via externally programmable pins, but they are fixed, internally mask programmed, for the KR9602.

Oscillator:

The main clocks are derived from either an external clock source or from the Internal oscillator. The resultant signal is then routed to a divider with a mask programmable division rate from 2 to 63. If no division is required then the divider is bypassed. The external clock requires one pin (pin #1), while the Internal oscillator needs three pins (pins #1, 2, 3) for frequency selection via an external resistor and capacitor.

Lockout/Rollover: LO/RO

This option selects the operation of the key scan when a new key is detected. In Lockout the scan stops as long as the key is down. In Rollover the scan stops till the new key is debounced by the DELAY CAP and the key code is output. Then the key position is marked as down and the scan continues until another new key is seen. The option is selected either by an external pin or internally mask programmed, fixed in either state. The external LOCKOUT selection is optionally hi or low active. A pull-down resistor to ground is optional.

Complement Control: CC

This option inverts the logic true state of the DATA OUT-

PIN	FUNCTION (input unless noted)
1	Ext clock (opt. internal divisor of 1-63)**
1	Pin 1 of Internal oscillator.
2	Pin 2 of Internal oscillator.
2	Lo/Ro CC CE ARD** ARO** AR1**
3	Pin 3 of Internal oscillator.
3	Lo/Ro CC CE ARD** ARO** AR1**
4	AKO output
4	Lo/Ro CC CE ARD** ARO** AR1**
5	AKO or B10 output
5	Lo/Ro CC CE ARD** ARO** AR1**
6	B9 or AKO** output

Options Available for the KR9602:

The following options can be obtained on the KR9602 only with a mask program, and are not pin selectable:

Lo/Ro, CC, AUTO-REPEAT, LONG DELAY, SHORT DELAY, CLOCK DIVISOR 1,2,4,8,16,32,63; PARITY, 1 OR 2 STOP BITS.

Legend

CC = COMPLEMENT CONTROL
 Lo/Ro = LOCKOUT/ROLLOVER
 B9 = B9 (DATA) OUTPUT
 INTERNAL CLOCK = SELF CONTAINED OSCILLATOR (Not available in KR9602)
 EXTERNAL CLOCK = EXTERNAL FREQUENCY SOURCE
 ARD = INITIAL AUTO-REPEAT DELAY
 ARO, AR1 = SECONDARY AUTO-REPEAT DELAY, OR NO AUTO-REPEAT WHEN BOTH ARE FALSE.

*Contact local sales office for custom coding sheet.
 **Not available on the KR9600.

PUTS and can optionally additionally invert the logic true state of the DATA READY pin. The option can be internally fixed as true or false where true will output a high logic level. When externally selected the option can be either input high or low active true. The pulldown to ground is optional.

Data Ready:

The data ready pin is optionally either a pulse or level upon an output state ready to transfer. This transfer occurs when a new key is encoded or when the current key is repeating via the repeat logic. This output is individually capable of being disabled via CE or inverted via CC. To invert DATA READY is to have the pulse go logic low or the level fall to logic low active when the output is allowed to drive out of the chip.

Any Key Down: AKO output

The AKO output is an indicator to tell that there is at least one key determined to be depressed. The output is optionally logic high or low true. The CE can be separately used to set the output in the high impedance mode. AKO will reset one full keyboard scan time after the last key is released. AKO cannot be inverted by CC (complement control).

Chip Enable: \overline{CE}

The chip enable option can be internally fixed to true or

can be externally selected. When an external pin is used the true level is only low true. The true state means that the outputs connected to CE will go to the driven state from the high-impedance condition. Output pins B1-B10 are always affected by Chip Enable (CE), optional for Data Ready and Any Key Down. A pulldown to ground is optional.

Shift Control Lock: S C L

These three pins determine what will be output in response to a new key being detected. The Caps Lock pin is optional on the KR9601 and KR9602 but it is not available on the KR9600. All three pins have optional pulldown resistors to ground. The Lock option is allowed if data bit nine of the ten data bits is programmed as true. In other words the Rom is read with no lock logic allowed, but with the full influence of the Shift and Control pins. This determines the B9 output which is used to see if this key can be shifted (be it a control code or not) by modifying the effect of the Shift upon a second read of the rom. The operation of the allowed Lock follows this table:

L	B9	S	C	Result	
F	F	F	F	N	
F	F	F	T	C	
F	F	T	F	S	L = CAPS LOCK
F	F	T	T	SC	B9 = DATA OUTPUT B9
F	T	F	F	N	N = NORMAL
F	T	F	T	C	S = SHIFT
F	T	T	F	S	C = CONTROL
F	T	T	T	SC	SC = SHIFT and CONTROL
T	F	F	F	N	
T	F	F	T	C	
T	F	T	F	S	
T	F	T	T	SC	
T	T	F	F	S	Force N->S allow shift (ie m->M)
T	T	F	T	SC	Force C->SC shift of Control
T	T	T	F	*S/N	Opt Force S->N allow reverse (ie M->m)
T	T	T	T	*SC/C	Opt Force SC->C remove shift in Shift-Control

*The mask programmable option for the removal of the shift is coded as either ON for all keys or OFF. Note that the B9 DATA output (and all the others) is the code of the second decode. Note that shift only occurs when both the lock is true and the unmodified code gives a B9 ROM output as true.

Repeat: ARD AR0 AR1

When the Auto-repeat option is selected and a key is pressed, either of two delays can be selected. Typically a long initial delay after the key is pressed, and short delays afterwards if the key is still pressed. These delays

consist of a programmable number of scan frequency time clocks varying from 2 to 131071 clock times.

This option is masked programmable and dependent on the programming of the data bit 10 of the ten data outputs to be true for the resultant key code (after lock logic) and upon whether any repeat action should occur at all.

There are three optional pins associated with the auto repeat logic: AR0, AR1, and ARD. Each of these can individually optionally have a pulldown resistor to ground. ARD controls the selection of the initial repeat delay count code, while the combination of AR0 and AR1 controls the selection of the short delays as shown below. If no external pins are desired then those functions can be mask programmed.

TYPICAL INITIAL REPEAT DELAY COUNTS

ARD = hi 80000 clock times
ARD = low 40000 clock times

The repeat delays are selected by a two bit code where one decode is used to disable the repeat operation completely.

TYPICAL SECONDARY REPEAT COUNTS

AR0	AR1	Count
0	0	All Auto-Repeat Disabled
0	1	6250
1	0	3125
1	1	1250

Typical Example:

One typical approach would be to mask program ARD for only one long delay value and mask AR0 to ground. This way one can save two option pins for ARD and AR0 and still be able to select or disable auto-repeat via AR1 and have the option of having one fixed short delay value.

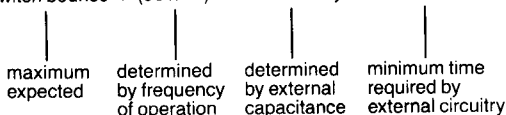
ROM Data:

The actual programming data is in 10 bit wide characters with four function codes for each key position. There are 90 key positions organized as 9 "X" outputs with 10 "Y" inputs. The four functions as previously defined are Control, Shift, Normal, and Shift-Control.

The use of the optional Lock requires the programming of the B9 data bit. The use of the optional Auto-Repeat requires the programming of the B10 data bit. If the B9 or B10 outputs are used then these will show the result of the contents of the "corrected" key function data bits. The "corrected" function is the possibly changed Normal to Shift etc. etc. so that the output is that of the 'Shifted key code' NOT that of the initial key code.

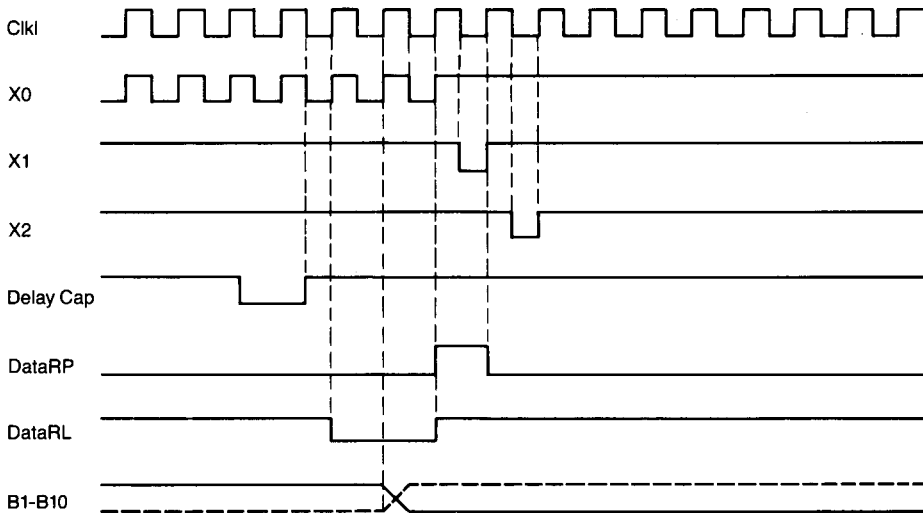
Minimum Switch Closure:

$$T = \text{Switch bounce} + (90 \times 1/f) + \text{Strobe delay} + \text{Strobe width}$$

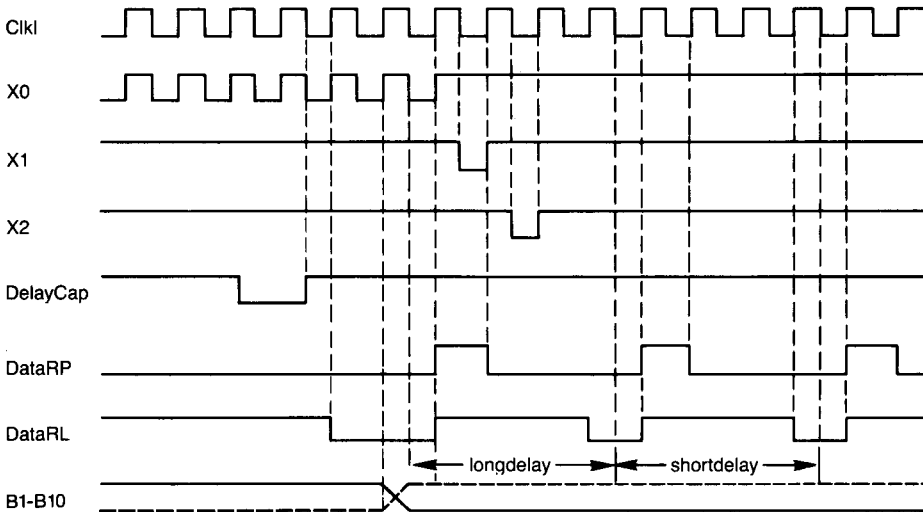


CONDITIONS:

The clock divider is 1 so that CkI1 is "same as clock IN".
A key is pressed down at X0Y0 but the delay cap has not timed out.
Data Ready is high true and we have already had another key.
DataRP = Data Ready as a Pulse DataRL = Data Ready as a Level



Condition: Test mode autorepeat at divide by 4 and keep key down



ELECTRICAL CHARACTERISTICS: KR9600, KR9601, KR9602

MAXIMUM GUARANTEED RATINGS

Operating Temperature Range**	0°C to +70°C
Storage Temperature Range	-55°C to +150°C
Lead Temperature (soldering, 10 sec.)	+325°C
Positive Voltage on any Pin, with respect to ground	+8.0V
Negative Voltage on any Pin, with respect to ground	-0.3V

ELECTRICAL CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = +5V ± 5%, unless otherwise noted)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	COMMENTS
D.C. CHARACTERISTICS						
INPUT VOLTAGE LEVELS						
Low Level	V _{IL}			0.8	V	All inputs
High Level	V _{IH}	2.0			V	Except Y + 16X CLK
		2.2			V	16X CLK only
Y INPUTS						
High Level	V _{YIH}	2.8			V	Y input
Low Level	V _{YIL}			0.8	V	Y input
INPUT CURRENT						
Leakage	I _L			10.0	μA	All inputs except Y V _{IN} = 5V
Input with Pull-down resistor selected as option Y inputs	I _{YIL}	75 -100	-400	220 -500	μA μA	V _{IN} = 5V V _{YIL} = 1 volt Y inputs only
OUTPUT VOLTAGE LEVELS						
Low Level	V _{OL}			0.4	V	I _{OL} = 1.6 mA
High Level	V _{OH}	2.4			V	I _{OH} = 100 μA
X output voltage	V _{OL} V _{OH}		0.4 4.0		V V	Except X outputs 600 μA clock high I _{OH} = 10 μA B1-B10
TRI-STATE LEAKAGE						
INPUT CAPACITANCE						
All inputs	C _{IN}			10	pF	Except Y inputs
POWER SUPPLY CURRENT						
	I _{CC}		20	40	mA	KR9600/01
	I _{CC}		15	35	mA	KR9602
A.C. CHARACTERISTICS						
CLOCK FREQUENCY*						
	F _{IN}	0.01		4	MHz	KR9601/02
		0.01		0.1	MHz	KR9600
		DC		640	KHz	KR9602
16X CLOCK FREQUENCY						
Chip enable access time	T _{CE}			250	ns	
SWITCH CHARACTERISTICS						
Min switch closure						see timing diagram
Contact closure resistance	Z _{CC} Z _{CC}			300	ohms	
		1 x 10 ⁷				

NOTE: The KR9600 is a direct replacement for the KR3600. Please note that due to the logic level of the KR9600, when replacing the KR3600 in a N-Key rollover system where diodes are utilized, the polarity of the diodes must be reversed.

* Divisor on KR9601/02 must be selected such that the resulting internal scan frequency is 10 KHz min to 100 KHz max.

** Parts optionally available in extended temperature ranges in hermetic packages. Inquire at factory.

KR9600-PRO DESCRIPTION

The KR9600 PRO is a MOS/LSI device intended to simplify the interface of a microprocessor to a keyboard matrix. Like the other KR9600 parts, the KR9600 PRO contains all of the logic to de-bounce and encode key-switch closures, while providing either a 2-key or N-key rollover.

The output of the KR9600 PRO is a simple binary code which may be converted to a standard information code by a PROM or directly by a microprocessor. This permits a user maximum flexibility of key layout with simple field programming.

The code in the KR9600 is shown in Table I. The format is simple: output bits, 9, 8, 7, 6, 5, 4 and 1 are a binary sequence. The count starts at X0, Y0 and increments through X0Y1, X0Y2...X8Y9. Bit 9 is the LSB; bit 1 is the MSB.

Bits 2 and 3 indicate the mode as follows:

Bit 2	Bit 3	
0	0	Normal
0	1	Shift
1	0	Control
1	1	Shift Control

For maximum ease of use and flexibility, an internal scanning oscillator is used, with pin selection of N-key lockout (also known as 2-key rollover) and N-key rollover. An "any-key-down" output is provided for such uses as repeat oscillator keying.

Figure 1 shows a PROM-encoded 64 key, 4 mode application, using a 256 x 8 PROM, and Figure 2 a full 90 key, 4 mode application utilizing a 512 x 8 PROM.

If N-key rollover operation is desired, it is recommended that a diode be inserted in series with each switch as shown. This prevents "phantom" key closures from resulting if three or more keys are depressed simultaneously.

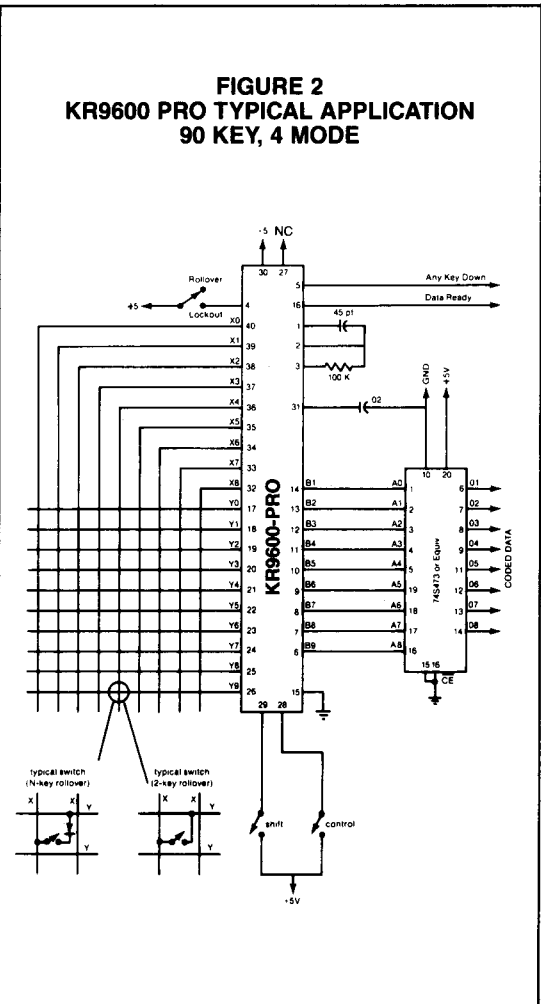
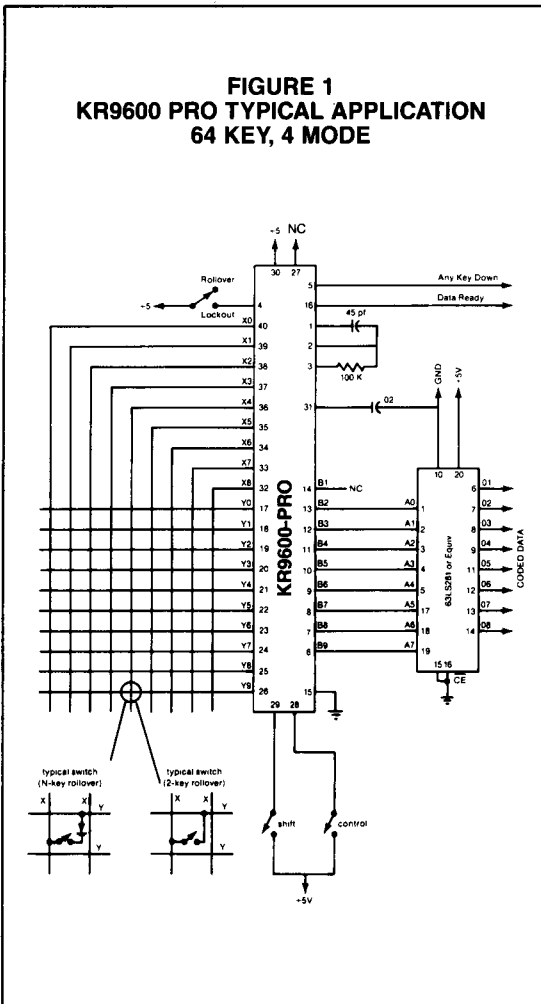


TABLE 1
KR9600-PRO CODING SHEET AND OPTIONS

XY	Normal	Shift	Control	Shift/Control
	B-12345678 910	B-12345678 910	B-12345678 910	B-12345678 910
00	00000000	00100000	01000000	01100000
01	00000001	00100001	01000001	01100001
02	00000010	00100010	01000010	01100010
03	00000011	00100011	01000011	01100011
04	00000100	00100100	01000100	01100100
05	00000101	00100101	01000101	01100101
06	00000110	00100110	01000110	01100110
07	00000111	00100111	01000111	01100111
08	00001000	00100100	01001000	01100100
09	00001001	00100101	01001001	01100101
10	00001010	00100110	01001010	01100110
11	00001011	00100111	01001011	01100111
12	00001100	00100100	01001100	01100100
13	00001101	00100101	01001101	01100101
14	00001110	00100110	01001110	01100110
15	00001111	00100111	01001111	01100111
16	00010000	00101000	01001000	01101000
17	00010001	00101001	01001001	01101001
18	00010010	00101010	01001010	01101010
19	00010011	00101011	01001011	01101011
20	00010100	00101100	01001100	01101100
21	00010101	00101101	01001101	01101101
22	00010110	00101110	01001110	01101110
23	00010111	00101111	01001111	01101111
24	00011000	00101100	01001100	01101100
25	00011001	00101101	01001101	01101101
26	00011010	00101110	01001110	01101110
27	00011011	00101111	01001111	01101111
28	00011100	00101100	01001100	01101100
29	00011101	00101101	01001101	01101101
30	00011110	00101110	01001110	01101110
31	00011111	00101111	01001111	01101111
32	00100000	00110000	01010000	01110000
33	00100001	00110001	01010001	01110001
34	00100010	00110010	01010010	01110010
35	00100011	00110011	01010011	01110011
36	00100100	00110100	01010100	01110100
37	00100101	00110101	01010101	01110101
38	00100110	00110110	01010110	01110110
39	00100111	00110111	01010111	01110111
40	00101000	00110100	01010100	01110100
41	00101001	00110101	01010101	01110101
42	00101010	00110110	01010110	01110110
43	00101011	00110111	01010111	01110111
44	00101100	00110100	01010100	01110100
45	00101101	00110101	01010101	01110101
46	00101110	00110110	01010110	01110110
47	00101111	00110111	01010111	01110111
48	00110000	00111000	01011000	01111000
49	00110001	00111001	01011001	01111001
50	00110010	00111010	01011010	01111010
51	00110011	00111011	01011011	01111011
52	00110100	00111100	01011100	01111100
53	00110101	00111101	01011101	01111101
54	00110110	00111110	01011110	01111110
55	00110111	00111111	01011111	01111111
56	00111000	00111100	01011100	01111100
57	00111001	00111101	01011101	01111101
58	00111010	00111110	01011110	01111110
59	00111011	00111111	01011111	01111111
60	00111100	00111100	01011100	01111100
61	00111101	00111101	01011101	01111101
62	00111110	00111110	01011110	01111110
63	00111111	00111111	01011111	01111111
64	10000000	10100000	11000000	11100000
65	10000001	10100001	11000001	11100001
66	10000010	10100010	11000010	11100010
67	10000011	10100011	11000011	11100011
68	10000100	10100100	11000100	11100100
69	10000101	10100101	11000101	11100101
70	10000110	10100110	11000110	11100110
71	10000111	10100111	11000111	11100111
72	10000100	10100100	11000100	11100100
73	10000101	10100101	11000101	11100101
74	10000110	10100110	11000110	11100110
75	10000111	10100111	11000111	11100111
76	10000100	10100100	11000100	11100100
77	10000101	10100101	11000101	11100101
78	10000110	10100110	11000110	11100110
79	10000111	10100111	11000111	11100111
80	10001000	10101000	11001000	11101000
81	10001001	10101001	11001001	11101001
82	10001010	10101010	11001010	11101010
83	10001011	10101011	11001011	11101011
84	10001100	10101100	11001100	11101100
85	10001101	10101101	11001101	11101101
86	10001110	10101110	11001110	11101110
87	10001111	10101111	11001111	11101111
88	10001100	10101100	11001100	11101100
89	10001101	10101101	11001101	11101101

OPTIONS:
Internal Oscillator (Pins 1, 2, 3)
Lockout/Rollover (Pin 4)
Internal Resistor to GND
Lockout is Logic 1

Pulse Data Ready
Any Key Down (Pin 5) Positive Output
Internal Resistor to GND on Shift
and Control Pins

CODING FOR KR9600-STD

	Normal B-12345678910	Shift B-12345678910	Control B-12345678910	Shift Control B-12345678910
00	1 100011001	< 001111001	1 100011011	SUB 010100001
01	q 100011010	Q 100010010	q 100011111	DLE 000010001
02	a 100001010	A 100000010	a 100001111	@ 000000101
03	z 010111010	Z 010110010	z 010111111	P 000010010
04	HT 100110000	HT 100100000	HT 100110000	100100010
05	H 000100010	H 000100010	H 000100010	H 000100111
06	+ 110101001	> 110101001	+ 110101001	+ 110101101
07	SC 011100100	> 011111001	SC 011100001	SC 011100001
08	p 000011010	@ 000001001	NUL 000000001	NUL 000000001
09	1 100011001	! 1000011001	SOH 100000001	SOH 100000001
10	2 010011001	@ 000000010	2 010011011	ETB 111010001
11	w 111010101	W 111010010	w 111011111	001100101
12	s 110011010	S 110010010	s 110011111	A 000000101
13	x 000111010	X 000110010	x 000111111	Q 100010101
14	RS 011100001	RS 011100001	% 101001001	FS 001100001
15	% 101001001	% 101001001	% 101001001	% 101001011
16	m 101101010	! 101100101	CR 101100001	CR 101100001
17	SI 111100001	SI 111100001	SI 111100001	SI 111100011
18	r 011101010	! 101100101	SC 011100001	SC 011100001
19	2 100011001	* 1000011001	STX 101000001	STX 010000001
20	3 110011001	# 1100011001	3 110011011	NAK 101010001
21	e 101001010	E 101000010	e 101001111	DC3 110010001
22	d 001001010	D 001000010	d 001011111	010000101
23	c 110001010	C 110000010	c 110011111	R 010010010
24	- 111110010	- 111110010	- 111110010	011110010
25	\$ 001001001	\$ 001001001	\$ 001001001	\$ 001001011
26	L 001100010	L 001100010	L 001100010	L 001100011
27	US 111100001	US 111100001	US 111100001	US 111100011
28	e 011011001	& 0110011001	ACK 011000001	ACK 011000001
29	k 101010101	! 101100101	DEL 111111101	DEL 111111101
30	k 001011001	\$ 0010011001	4 001011011	DC4 001000010
31	r 010011010	R 010001010	r 010011111	ENQ 101000001
32	f 010001010	F 010000010	f 010001111	C 110000010
33	SP 000001000	SP 000001000	SP 000001000	SP 000001000
34	CAN 000110100	CR 0001101000	CAN 000110000	BS 000100000
35	CR 101100001	CR 101100001	CR 101100001	M 101100010
36	110111101	110111101	110111111	K 110100010
37	VT 110100000	V 110100000	VT 110100000	VT 110100001
38	7 111011001	! 1110011001	BEL 111000001	BEL 111000001
39	0100011001	! 0100011001	* 0100011001	* 010001101
40	s 101011001	% 1010011001	5 101011011	STX 010000001
41	l 001011010	T 001010010	l 001011111	E 010100011
42	g 111001010	! 111000010	G 111001111	D 001000010
43	v 011011010	V 011010010	v 011011111	S 110010010
44	ETX 110000000	ETX 110000000	ETX 110000001	ETX 110000001
45	101111101	! 101111101	! 101111101	N 011100010
46	111111100	! 111111100	! 111111011	! 110100101
47	- 101101001	- 101111001	- 101101001	- 101101011
48	! 100101001	! 100101001	! 100101001	! 100101011
49	SP 000001001	SP 000001001	SP 000001001	SP 000001011
50	e 011011001	> 011111001	e 011011011	SOH 100000001
51	y 100110101	Y 100110010	y 100111111	DC1 100100001
52	h 000101001	H 000100010	h 000101111	E 010100011
53	b 010001010	B 010000010	b 010001111	T 001010010
54	* 011110001	* 010110001	* 011110011	SYN 011010001
55	> 011110001	> 011110001	> 011110011	Z 010110010
56	+ 110111001	+ 110101001	+ 110111011	Y 001100010
57	NUL 000000001	NUL 000000001	NUL 000000001	NUL 000000001
58	010101001	* 010101001	* 010101001	* 010101011
59	! 100001001	! 100001001	! 100001001	! 100001011
60	7 111011001	& 0110011001	7 111011011	ETX 110000001
61	u 101010101	U 101010010	u 101011111	BEL 111000001
62	j 010101010	J 010100010	j 010101111	F 011000010
63	n 011101010	N 011100010	n 011101111	U 101010010
64	= 101111000	= 101111000	= 101111010	= 011111100
65	< 001111001	< 001111001	< 001111011	W 111010010
66	p 000011010	P 000010010	p 000011111	J 010100010
67	0 000011001	! 100101001	0 000011010	DC2 010000001
68	& 011001001	& 011001001	& 011001001	& 011001011
69	# 110001001	# 110001001	# 110001001	# 110001011
70	8 000111001	* 010101001	8 000111011	ESC 110100001
71	l 100101010	! 100100010	l 100101111	ACK 011000001
72	k 110101010	K 110100010	k 110101111	G 111000010
73	m 101101010	M 101100010	m 101101111	V 011010010
74	/ 111011001	? 111111001	/ 111011001	/ 111001001
75	/ 111001001	? 0100011001	/ 111001001	? 010001001
76	LF 010100000	LF 010100000	LF 010100000	GS 101100000
77	= 101111001	+ 110101001	= 101111001	+ 110101001
78	FF 001100100	< 001111001	FF 001100001	FF 001100011
79	(000101001	(000101001	(000101001	(000101011
80	9 100111001	(000101001	9 100111011	EM 100110001
81	o 111010101	O 111000101	o 111010111	111100101
82	l 001101010	L 001100010	l 001101111	X 000110010
83	. 001101001	. 001101001	. 001101001	. 001101011
84	> 011101001	> 011101001	> 011101001	> 011101011
85	110111001	! 110111001	! 110111001	! 110111001
86] 101100101] 110110010] 101100101] 110100101
87	- 110101001	- 111100101	- 110101001	- 111100101
88	0 000011001	0 000011001	0 000011001	0 000011001
89	9 100111001	! 100101001	HT 100100001	HT 100100001

OPTIONS:
 Internal Oscillator (Pins 1, 2, 3)
 Any Key Down (Pin 4) Positive Output
 N-Key Rollover only
 Pulse Data Ready signal

Internal Resistor to GND on Shift and Control Pins
 KR9600-STD outputs provides ASCII bits 1-6 on B1-B6, and bit 7 on B8

SECTION VIII

CODING FOR KR9601 AND KR9602 STD

XY	Normal B-12345678 910	Shift B-12345678 910	Control B-12345678 910	Shift/Control B-12345678 910
00	00000001 00	01010101 00	10101001 00	10101001 00
01	00000010 01	01010110 01	10101010 01	10101010 01
02	00000011 01	01010111 01	10101011 01	10101011 01
03	00000100 01	01011000 01	10101100 01	10101100 01
04	00000101 01	01011001 01	10101101 01	10101101 01
05	00000110 01	01011010 01	10101110 01	10101110 01
06	00000111 01	01011011 01	10101111 01	10101111 01
07	00001000 01	01011100 01	10110000 01	10110000 01
08	00001001 01	01011101 01	10110001 01	10110001 01
09	00001010 01	01011110 01	10110010 01	10110010 01
10	00001011 01	01011111 01	10110011 01	10110011 01
11	00001100 01	01100000 01	10110100 01	10110100 01
12	00001101 01	01100001 01	10110101 01	10110101 01
13	00001110 01	01100010 01	10110110 01	10110110 01
14	00001111 01	01100011 01	10110111 01	10110111 01
15	00001100 01	01100010 01	10110100 01	10110100 01
16	00001111 01	01100011 01	10110110 01	10110110 01
17	00010000 01	01100100 01	10111000 01	10111000 01
18	00010001 01	01100101 01	10111001 01	10111001 01
19	00010010 01	01100110 01	10111010 01	10111010 01
20	00010011 01	01100111 01	10111011 01	10111011 01
21	00010100 01	01101000 01	10111100 01	10111100 01
22	00010101 01	01101001 01	10111101 01	10111101 01
23	00010110 01	01101010 01	10111110 01	10111110 01
24	00010111 01	01101011 01	10111111 01	10111111 01
25	00011000 01	01101100 01	10000000 01	10000000 01
26	00011001 01	01101101 01	10000001 01	10000001 01
27	00011010 01	01101110 01	10000010 01	10000010 01
28	00011011 01	01101111 01	10000011 01	10000011 01
29	00011100 01	01110000 01	10000100 01	10000100 01
30	00011101 01	01110001 01	10000101 01	10000101 01
31	00011110 01	01110010 01	10000110 01	10000110 01
32	00011111 01	01110011 01	10000111 01	10000111 01
33	00011100 01	01110000 01	10000100 01	10000100 01
34	00100000 01	01110100 01	10001000 01	10001000 01
35	00100001 01	01110101 01	10001001 01	10001001 01
36	00100010 01	01110110 01	10001010 01	10001010 01
37	00100011 01	01110111 01	10001011 01	10001011 01
38	00100100 01	01110100 01	10001100 01	10001100 01
39	00100101 01	01110101 01	10001101 01	10001101 01
40	00100110 01	01110110 01	10001110 01	10001110 01
41	00100111 01	01110111 01	10001111 01	10001111 01
42	00101000 01	01111000 01	10010000 01	10010000 01
43	00101001 01	01111001 01	10010001 01	10010001 01
44	00101010 01	01111010 01	10010010 01	10010010 01
45	00101011 01	01111011 01	10010011 01	10010011 01
46	00101100 01	10000000 01	10010100 01	10010100 01
47	00101101 01	10000001 01	10010101 01	10010101 01
48	00101110 01	10000010 01	10010110 01	10010110 01
49	00101111 01	10000011 01	10010111 01	10010111 01
50	00101100 01	10000000 01	10010100 01	10010100 01
51	00110000 01	10000100 01	10011000 01	10011000 01
52	00110001 01	10000101 01	10011001 01	10011001 01
53	00110010 01	10000110 01	10011010 01	10011010 01
54	00110011 01	10000111 01	10011011 01	10011011 01
55	00110100 01	10000100 01	10011100 01	10011100 01
56	00110101 01	10000101 01	10011101 01	10011101 01
57	00110110 01	10000110 01	10011110 01	10011110 01
58	00110111 01	10000111 01	10011111 01	10011111 01
59	00111000 01	10001000 01	11000000 01	11000000 01
60	00111001 01	10001001 01	11000001 01	11000001 01
61	00111010 01	10001010 01	11000010 01	11000010 01
62	00111011 01	10001011 01	11000011 01	11000011 01
63	00111100 01	10001100 01	11000100 01	11000100 01
64	00111101 01	10001101 01	11000101 01	11000101 01
65	00111110 01	10001110 01	11000110 01	11000110 01
66	00111111 01	10001111 01	11000111 01	11000111 01
67	00111100 01	10001000 01	11000100 01	11000100 01
68	00111101 01	10001001 01	11000101 01	11000101 01
69	00111110 01	10001010 01	11000110 01	11000110 01
70	01000000 01	10010000 01	11010000 01	11010000 01
71	01000001 01	10010001 01	11010001 01	11010001 01
72	01000010 01	10010010 01	11010010 01	11010010 01
73	01000011 01	10010011 01	11010011 01	11010011 01
74	01000100 01	10010000 01	11010100 01	11010100 01
75	01000101 01	10010001 01	11010101 01	11010101 01
76	01000110 01	10010010 01	11010110 01	11010110 01
77	01000111 01	10010011 01	11010111 01	11010111 01
78	01001000 01	10011000 01	11011000 01	11011000 01
79	01001001 01	10011001 01	11011001 01	11011001 01
80	01001010 01	10011010 01	11011010 01	11011010 01
81	01001011 01	10011011 01	11011011 01	11011011 01
82	01001100 01	10100000 01	11100000 01	11100000 01
83	01001101 01	10100001 01	11100001 01	11100001 01
84	01001110 01	10100010 01	11100010 01	11100010 01
85	01001111 01	10100011 01	11100011 01	11100011 01
86	01010000 01	10100100 01	11100000 01	11110000 01
87	01010001 01	10100101 01	11100001 01	11110001 01
88	01010010 01	10100110 01	11100010 01	11110010 01
89	01010011 01	10100111 01	11100011 01	11110011 01

OPTIONS FOR THE KR9601-STD:

- PINS 1, 2, 3 INTERNAL OSCILLATOR [Input clock divisor = 1]
- PIN 4 CE [Active Low]
- PIN 5 AR1 [AR0 fixed at Lo = 0]
[FIXED LONG DELAY OF 40000 CLOCK TIMES]
[FIXED SHORT DELAY OF 6250 CLOCK TIMES]
- PIN 6 AKO [positive true]

Pulsed DATA READY signal

N-KEY ROLLOVER

Pull-down resistor to ground at the following pins:

- SHIFT
- CONTROL
- CAPS-LOCK
- ARO

OPTIONS FOR THE KR9602-STD:

N-KEY ROLLOVER

AUTO-REPEAT

[FIXED LONG DELAY OF 40000 CLOCK TIMES]
[FIXED SHORT DELAY OF 6250 CLOCK TIMES]

1 STOP bit.

No PARITY bit.

Input clock divisor of 63

Pull-down resistor to ground at the following pins:

- SHIFT
- CONTROL
- CAPS-LOCK

CODING FOR KR9602-012 (ASCII)

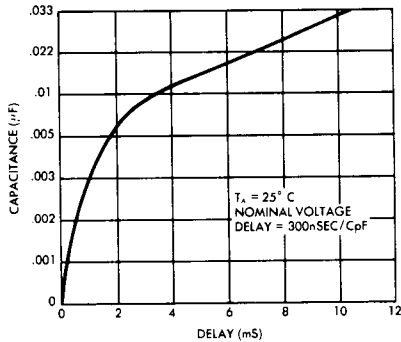
XY	Normal B-12345678910	Shift B-12345678910	Control B-12345678910	Shift Control B-12345678910
00	0000110001	1001010001	0000110001	1001010001
01	1001110001	0001010001	1001110001	0001010001
02	0001110001	0101010001	0001110001	0101010001
03	1110110001	010010001	1110110001	010010001
04	0110110001	0111101001	0110110001	0111101001
05	1010110001	1010110001	1010110001	1010110001
06	0010110001	0010010001	0010110001	0010010001
07	1100110001	1100010001	1100110001	1100010001
08	0100110001	0000010001	0100110001	0000010001
09	1000110001	1000110001	1000110001	1000110001
10	0001000001	0001000001	0001000001	0001000001
11	1010110001	1101010001	1011110001	1101010001
12	101010001	1111101001	111100001	111100101
13	1010101001	1010111001	1011100001	101010101
14	1101101001	1101111001	1101100000	110110100
15	1111011011	0000101011	0000100011	000010111
16	1111011011	1111001011	1111000011	1111000111
17	1001011011	1001001011	1001000011	100100111
18	1010111011	1010101011	1010100011	101010111
19	1001111011	1001101011	1001100011	100111011
20	0010111011	0010101011	0010100011	001010111
21	0100111011	0100101011	0100100011	010010111
22	1010011011	1010001011	1010000011	101000111
23	1110111011	0101001011	1110100011	111010011
24	1000111011	1000101011	1000100011	100010111
25	1101100000	1101100000	1101100000	1101100000
26	1001000001	1001000011	1001000001	1001000101
27	1011000001	1011000001	1011000001	1011000001
28	0000011001	0111111001	0000011001	0111111001
29	1110010001	0100010001	1110010001	0100010001
30	0011011011	010110001	110110001	010110001
31	1101011011	0011001011	0011000011	001100111
32	1101011011	1101001011	1101000011	110100111
33	0101011011	0101001011	0101000011	010100111
34	0001011011	0001001011	0001000011	000100111
35	1110011011	1110001011	1110000011	111000111
36	0110011011	0110001011	0110000011	011000111
37	0010011011	0010001011	0010000011	001000111
38	1000110111	1100101011	1100100011	110010111
39	1000011011	1000010111	1000000111	100000111
40	1111010001	111110001	1111000011	111110001
41	0111010001	011110001	0111000011	011110001
42	0011010001	001110001	0011000011	001110001
43	1011011011	1011001011	1011000011	101110011
44	0111011011	0111001011	0111000011	011100111
45	0100011011	0100001011	0100000011	010000111
46	0110111011	0110101011	0110100101	011010111
47	1100011011	1100001011	1110100101	110000111
48	0001100011	0001100011	0001100101	000110011
49	0101110111	0101101011	0101100011	010110111
50	0011101001	0011110001	0011100001	0011100101
51	0000010001	0000010001	0000010001	0000010001
52	1010000001	1010000001	1010000001	1010000001
53	0110000001	0110000001	0110000001	0110000001
54	1110000001	1110000001	1110000001	1110000001
55	1001000001	1001000001	1001000001	1001000001
56	0101000001	0101000001	0101000001	0101000001
57	1101000001	1101000001	1101000001	1101000001
58	0111000001	0111000001	0111000001	0111000001
59	1111000001	1111000001	1111000001	1111000001
60	0000100001	0000100001	0000100001	0000100001
61	1000100001	1000100001	1000100001	1000100001
62	0100100001	0100100001	0100100001	0100100001
63	1100100001	1100100001	1100100001	1100100001
64	0010000001	0010000001	0010000001	0010000001
65	1010100001	1010100001	1010100001	1010100001
66	0110100001	0110100001	0110100001	0110100001
67	1110100001	1110100001	1110100001	1110100001
68	0001100001	0001100001	0001100001	0001100001
69	1001100001	1001100001	1001100001	1001100001
70	0101100001	0101100001	0101100001	0101100001
71	0011100001	0011100001	0011100001	0011100001
72	1011100001	1011100001	1011100001	1011100001
73	0111100001	0111100001	0111100001	0111100001
74	1111100001	1111100001	1111100001	1111100001
75	0000000001	0000000001	0000000001	0000000001
76	1000000001	1000000001	1000000001	1000000001
77	0100000001	0100000001	0100000001	0100000001
78	1100000001	1100000001	1100000001	1100000001
79	0010000001	0010000001	0010000001	0010000001
80	000010111	000010111	000010111	000010111
81	1001110111	1001110111	1001110111	1001110111
82	0001110011	0001110011	0001110011	0001110011
83	1110110111	1110110111	1110110111	1110110111
84	1100100011	0110110011	1100100011	0110110011
85	1010110111	1010110011	1010110111	1010110011
86	0101010011	0101011011	0101010011	0101011011
87	1100110111	1100110011	1100110111	1100110011
88	0010100011	0100110011	0010100011	0100110011
89	1000110011	1000110011	1000110111	1000110011

OPTIONS FOR THE KR9602-012 ASCII:

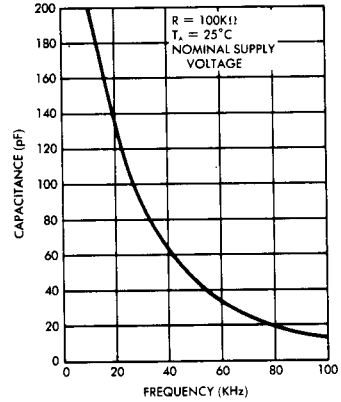
Lockout
 Auto Repeat
 (Fixed Long Delay of 60,000 Clock Times)
 (Fixed Short Delay of 2000 Clock Times)
 One Stop Bit
 Input Clock Divisor of 32

No Parity
 Eight Data Bits
 Pull down Resistor to Ground is at the following pins:
 — SHIFT
 — CONTROL
 — CAPS LOCK

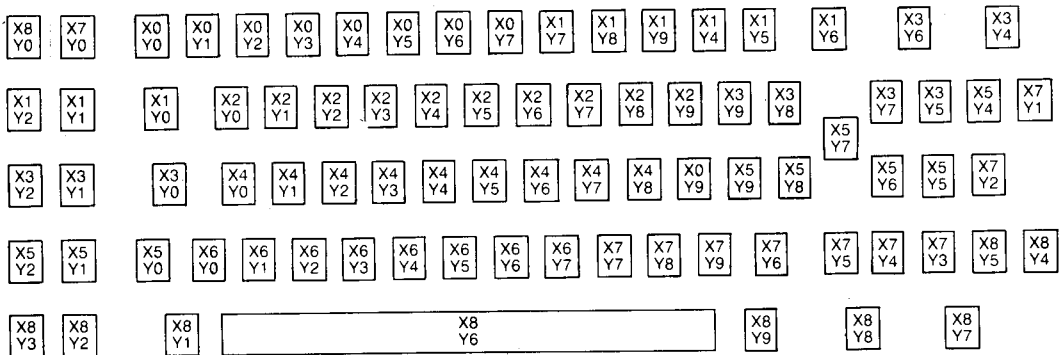
STROBE DELAY vs C2 FOR KR9600/1/2



OSCILLATOR FREQUENCY vs C1 FOR KR9600/KR9601



KEYBOARD LAYOUT FOR KR9601/9602-STD



STANDARD MICROSYSTEMS CORPORATION

35 Marcus Blvd. Hauppauge, NY 11786
(516) 273-3100 FAX: 516-227-8899

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