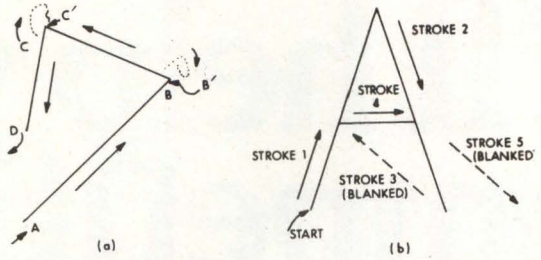


Constant vector intensity of Megatek's Whizzard graphic system is produced by turning off beam precisely as it passes through B. Beam continues on in undefined manner (a) and finally settles at point B'. After appropriate set-up time, beam begins from B' and moves toward C. As it passes precisely through B, beam is unblanked and vector is drawn toward C where cycle repeats. Stroke generated characters (b) take advantage of precision of vector generator, producing readable characters even at sizes below 0.1 in

monitor provides up to five colors in 16 bits of user definable, user programmable line texture. Any line texture may be blanked, doubling the total line texturing capacity of the system.

Hardcopy output is facilitated by a vector to raster converter implemented in hardware. The Rastorizer™ processes vectors, randomly converting from an unordered vector list into raster bit data for the plotter, eliminating the need for the host to order vectors prior to printing.

An interactive total refresh graphic system, 5000 series standalone and terminal configurations are compatible with Data General RDOS, DOS, and RTOS operating systems. The system has a self contained NOVA or ECLIPSE with 32k-words memory, dual floppy disc drive, and RS-232 interface.

The dual board MG552 graphic display unit uses hardware routines to speed vector processing and minimize host processing time. As a DMA device the graphic display unit receives coordinates directly from the computer's memory. Precise analog stroke writing offers typical endpoint matching and closure of 0.005" (0.0127 cm), 16 levels of intensity control, and constant vector intensity.

Circle 401 on Inquiry Card

Magnetic Tape Formatter Adapts GCR To Use With Minicomputers

The F6250 intelligent formatter carries out magnetic tape drive management and GCR/PE encoding and decoding, enabling group coded recording to be used with minicomputers. By incorporating this formatter, Pertec Computer Corp, Pertec Div, 9600 Irondale, Chatsworth, CA 91311, was able to simplify the system sufficiently to meet use and service needs of the minicomputer market.

An important feature of the maintenance concept is the simplicity of the I/O structure. Most tape dependent functions have been built into the formatter, relieving the host CPU and magnetic tape controller of considerable demands. The formatter interface communicates with the host CPU over a 28-line bus: a 16-bit control/status/data bidirectional bus, five common address space address lines, and six handshake control lines.

Three-level self-diagnostics allow troubleshooting without outside test equipment. Subsystem operation can be verified at the formatter panel keyboard in offline mode independent of external test equipment. First level diagnostic operation supplies the CPU with a continuous performance report and alerts it in the event of fault. A second level, offline mode, allows self test routines to be called by the technician to verify individual module integrity. The formatter's microprocessor executes these test routines stored in internal memory, po'ling individual microsequences associated with each module as test patterns are routed through the module to verify proper handling. The third level uses the CPU in a dedicated diagnostic mode and provides approximately 50 interface test messages. The first part of this diagnostic verifies the CSD bus/CAS memory interface and formatter control path. The second part checks the various modules, submodules, and individual circuits of the formatter.

Circle 402 on Inquiry Card

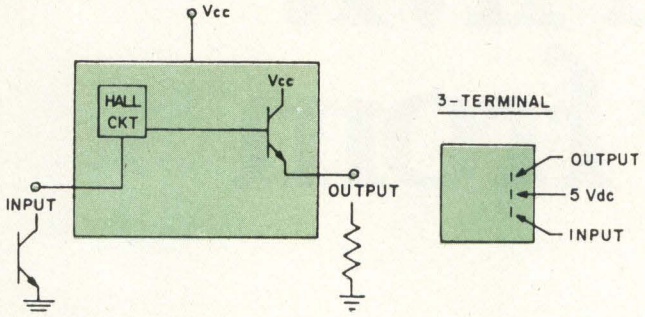
3-Terminal Module Reduces Current Drain For Standard Keyboard

A 3-terminal Hall effect keyboard module combined with an integral microcomputer reduces current drain for a standard 64-module keyboard by 140 mA. Replacing the customary 4-terminal module to achieve the 60% reduction in current, the 3T module was developed by Micro Switch Div, Honeywell, Inc, 11 W Spring St, Freeport, IL 61032, as a logical outgrowth of the keyboard's microcomputer capabilities.

In the 3T module the input terminal also serves as a minus supply connection. The module integrates with the onboard microcomputer's scan capabilities permitting application of power to only eight key modules at a time during a scan cycle.

Additional production economies are offered by the reduced size of the 3T Hall effect chips, helping to hold the line on prices without affecting traditional features and performance. The modules use the same variety of keytops provided since the Hall effect keyboards were introduced. Yet power requirements are reduced from the 1 A specified for a typical 64-key device to the 140 mA specified for keyboards using the 3T modules.

Other economies that are incorporated in the keyboards are materials that permit use of a punchable single

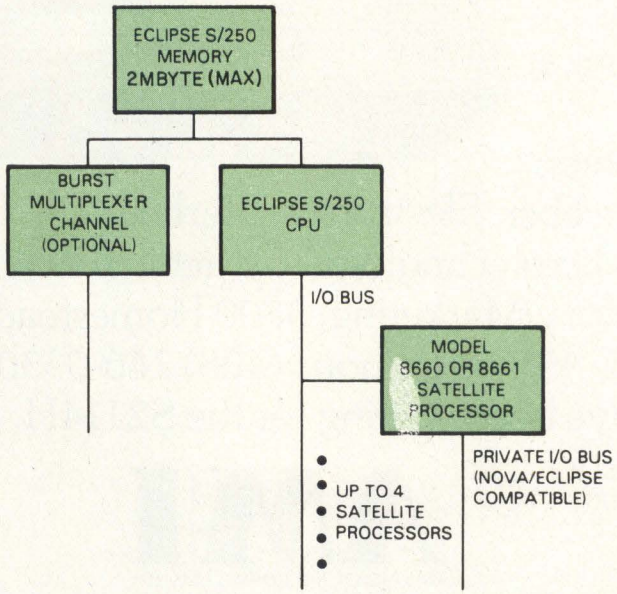


3-terminal Hall effect scan module from Honeywell's Micro Switch Div combines with keyboard's integral microcomputer, permitting power to be applied to only eight key modules at one time thereby reducing power requirements of keyboard by 60%

sided PC board. Automatically inserted jumper wires allow the manufacturer to keep all circuitry on one side of the board. Silk screening of component locations on the board facilitates assembly and field servicing.

Circle 403 on Inquiry Card

Satellite Processors Increase Computer's Processing Capabilities



Data General's satellite processors models 8660 and 8661 are configured on S/250 data channel and act as CPU I/O device, offloading host. Each has its own independent I/O bus for programmed I/O and data channel transfers, and supports cross-interrupt facility with host for interprocessor synchronization

Satellite processors models 8660 and 8661, optional peripheral processing units, increase the processing capabilities of ECLIPSE S/250 processors (see *Computer Design*, Oct 1978, p 30) from Data General Corp, Rt 9, Westboro, MA 01581. The units operate as frontend or independent processors significantly offloading the CPU. Both include two circuit boards of independent processor logic, memory and I/O buses, and implement the standard ECLIPSE instruction set with powerful extensions.

General purpose satellite processor model 8600 consists of 64k bytes of parity MOS with memory allocation and protection (MAP) capability, a microprogrammed processor with 200-ns cycle time, an independent CPU compatible I/O bus, software controllable console, and interface for bidirectional data transfer between S/250 and satellite processor. The satellite's instruction set consists of the basic ECLIPSE set plus character instruction set that facilitates bit, byte, and data string manipulation and translation.

Model 8661 with a fast hardware array processing extension consists of 56k bytes of parity MOS memory and MAP, 8k bytes of high speed bipolar array processing memory, processor logic, I/O bus, and S/250 interface. Array processing instructions common to the HP/130 and the CPU's integral array processor option are added to the basic ECLIPSE instruction set.

Configured on the S/250 high speed data channel, the satellite processors act as I/O devices. Each has its own independent I/O bus for programmed I/O and data channel transfers. Both support a cross interrupt facility with the S/250 for interprocessor synchronization.

Using MAP software control, the satellites direct memory reference instructions in the satellite program to local memory or to the host S/250 main memory. This facility also exists for data channel DMA references from devices on the satellite's private I/O bus, permitting both high speed interprocessor data transfer as well as enabling data sharing and routing.

Software supports the enhanced system for realtime event-driven and interactive environments. Tasks running under RDOS in the S/250 can bidirectionally communicate and transfer data with tasks running under RTOS in the satellite processor. Programs can be written in global